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Technical Note

1967-10

Operational Low-Power, Low- to High-Frequency Digital Circuit Elements: Refinements, Characteristics and Developments

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Lincoln Laboratory
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Lexington, Massachusetts

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

OPERATIONAL LOW-POWER, LOW- TO HIGH-FREQUENCY DIGITAL CIRCUIT ELEMENTS: REFINEMENTS, CHARACTERISTICS AND DEVELOPMENTS

D. E. CHACE

Group 63

TECHNICAL NOTE 1967-10

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LEXINGTON MASSACHUSETTS

ABSTRACT

This report contains various configurations of operational low-power digital circuit elements which have been refined and/or developed to carry out many functional requirements of digital system designs. Although they are primarily intended for use in space-oriented digital system applications, e.g., the Lincoln Experimental Satellite (LES) program, the configurations need not be limited to this purpose.

Characteristic operational data are included in all cases to point out various circuit requirements, capabilities and limitations.

A myriad of flip-flop configurations is provided to promote efficient systems design in regards to power consumption, noise immunity and cost.

Section IV covers some design considerations relating to high-speed, low-power flip-flop development.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

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OPERATIONAL LOW-POWER, LOW- TO HIGH-FREQUENCY DIGITAL CIRCUIT ELEMENTS: REFINEMENTS, CHARACTERISTICS AND DEVELOPMENTS

I. INTRODUCTION

Gates, along with various configurations of flip-flops, are probably the two most widely used circuit elements that go toward building a digital system. Design philosophies vary greatly, depending on the application and environment in which the system will operate. Circuit elements dealt with here center around a space environment application, or are adaptable to any other purpose, requiring these (as well as other) general considerations: reliability, long life, noise immunity, conservation of power, justification of packaging space usage, and immunity to inter-environment and ultimate environment physical hazards.

Although most of the circuits contained herein are not bold diversions from tried and true forms, an attempt has been made to define these forms in a manner that categorically confines their function and usage. For efficiency considerations in digital system designs for space applications, it is apparent that a degree of editing is in order regarding circuit capability vs need. That is to say, a circuit need not have a capability very much greater than required for its intended use. In most instances circuit capability, to a large degree, determines practical considerations such as the number and type of components required, the relative cost of these components, the space required to accommodate the circuit package, standby and operational power consumption, and time spent in development and testing. If sound editing of circuit capability vs need is accomplished, this will help contribute to an overall saving in the above mentioned areas.

This line of circuit elements is intended to provide a user with a variety of functional system components from which, based upon capability required, he may choose. The circuits outlined in this report are being integrated into digital systems in the Lincoln Experimental Satellite program beginning with LES-6. Placed upon these systems is an operational requirement covering many frequency domains from less than 1 Hz to over 10 MHz. It is therefore

apparent why similar function circuits that fall into capability categories are necessary, not only to conserve power but to contribute to net system efficiency.

Designs are based upon use-tested reliable practices, with refinements added to promote predictable operational results with categorical usage as a design guide. Characteristic operational information and specific data have been collected through extensive dynamic testing under conditions of a temperature environment. All listed data were collected at approximately +25°C, and variances at extreme low temperatures would not be unexpected.

II. COMPLEMENTARY CIRCUITS

Whenever high-frequency square waves or pulse waveforms are to be generated, it is mandatory that rise, fall, storage and transition times be kept at a minimum relative to the operational frequency being used. Single-stage saturated switches, either PNP or NPN, both suffer from the effects of storage time which results in slow fall or rise time, respectively.

The complementary circuits to follow overcome these effects for applications where higher speeds and faster edges are required. Transistors are arranged in a circuit so that they mutually supply each others lack, resulting in a push-pull saturated switching circuit operating in mutual harmony.

Figures 1 and 2 describe the storage effects encountered with single-stage saturated PNP or NPN switches.

In Fig. 3, a circuit arrangement using complementary connected transistors is shown whereby the storage effect produced previously is essentially completely overcome. This configuration adapts very well to custom biasing which is an important design factor, particularly when used for space system applications, because of the ever present power limitations. By adjusting the bias current resistively in the base networks, many combinations of bias voltage can be obtained which serve to adjust input sensitivity and/or output drive capability.

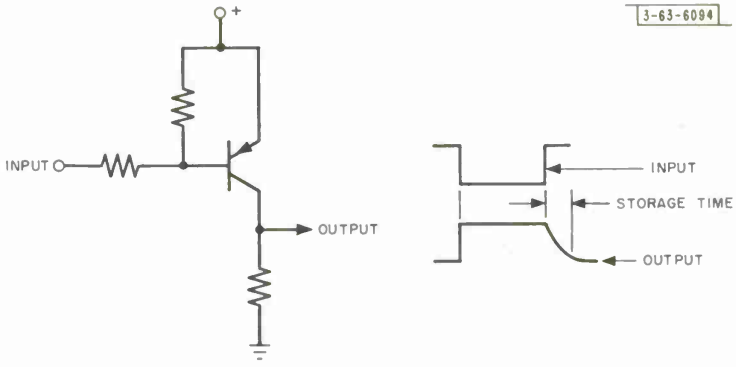


Fig. 1. Typical single-stage PNP storage effects.

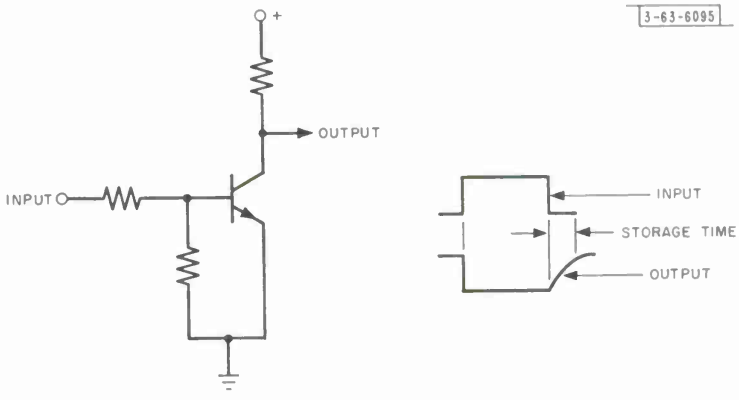


Fig. 2. Typical single-stage NPN storage effects.

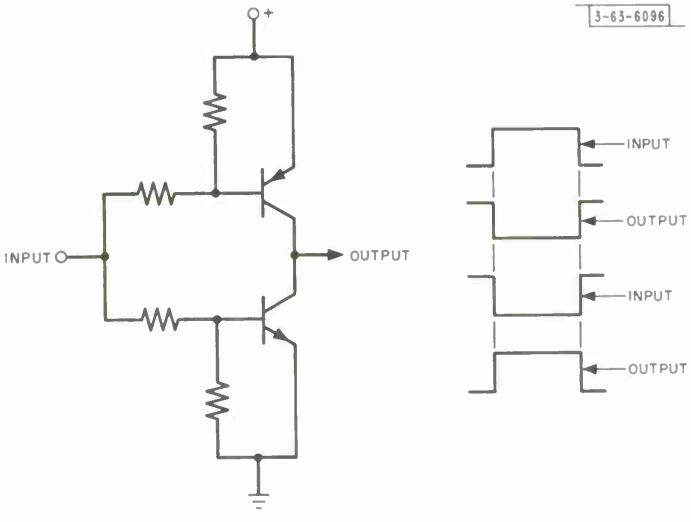
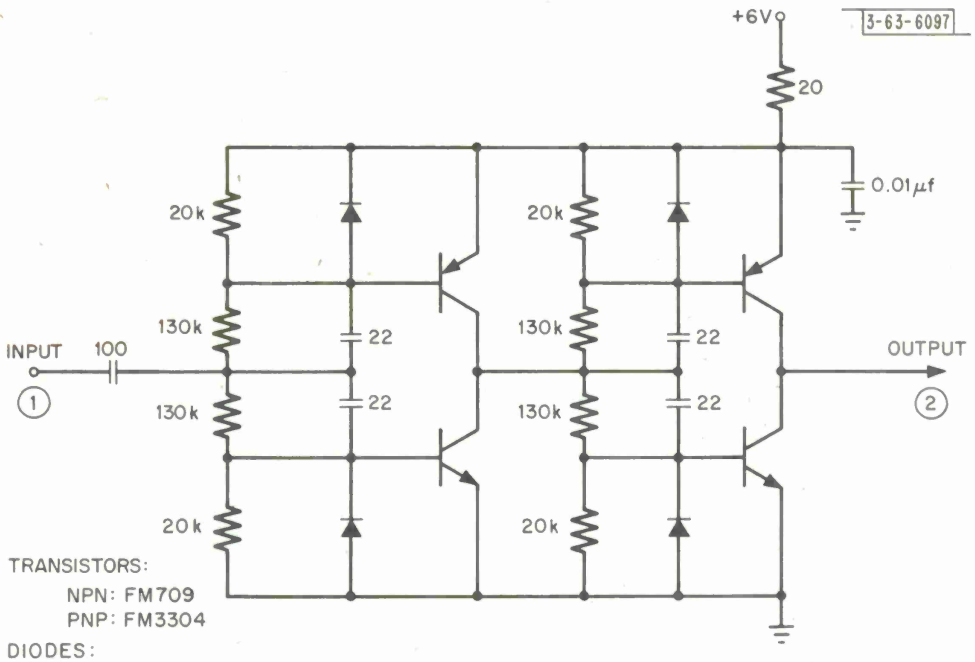


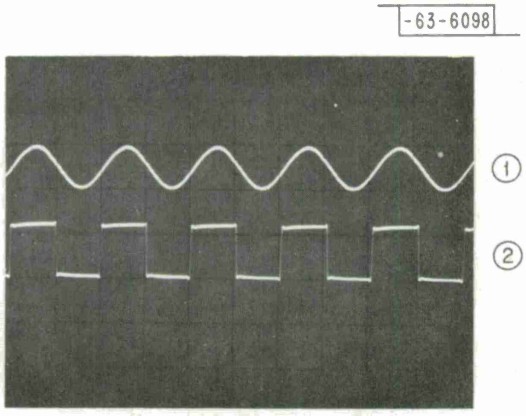
Fig. 3. Typical complementary output overcoming storage effects.

Circuit: Slicer #5821

Operational Capabilities:	
Frequency range	200 kHz to ⩾10 MHz
Temperature range	⩾±50°C
Supply voltage variation	⩾±30 percent
Input Requirements:	
Sinewave	⩾4 volts $\overline{pp}$
Output Characteristics:	
Rise time	<10 nsec
Fall time	<10 nsec
Levels	≈0 and +6 volts
Other Characteristics:	
Power consumption	1.8 mW at 1 MHz



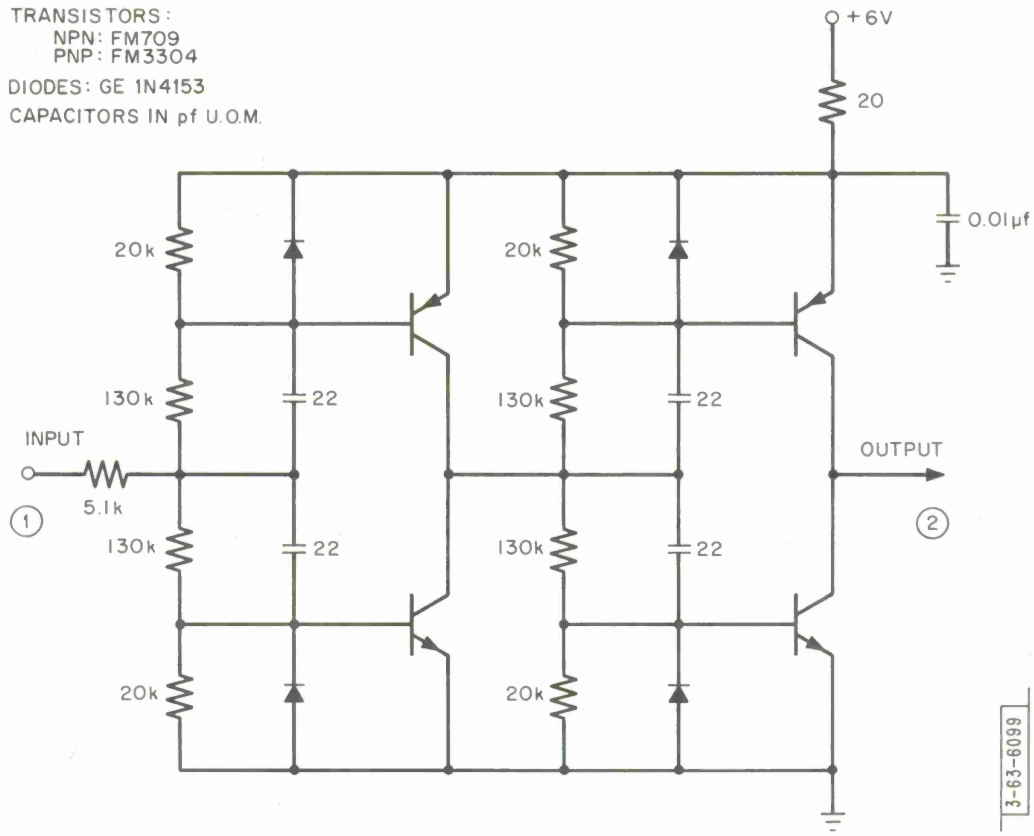
CIRCUIT DIAGRAM 1 (Slicer)
MODULE #5821



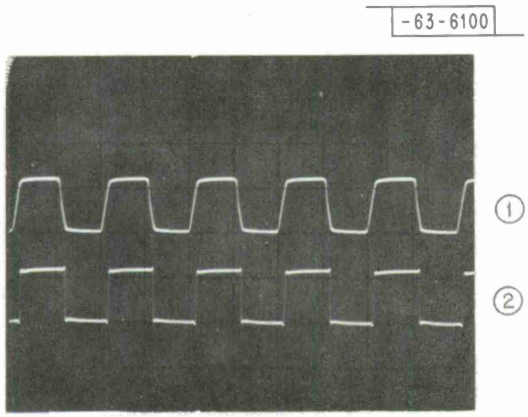
HORIZONTAL: 0.5 μsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 1 MHz

Circuit: Buffer Driver #5811

Operational Capabilities:	
Frequency range	0 to $\geq$5 MHz
Temperature range	$\geq \pm 50°C$
Supply voltage variation	$\geq \pm 30$ percent
Input Requirements:	
Pulse amplitude	$\geq$4 volts
Pulsewidth	$\geq$0.2 μsec
Output Characteristics:	
Rise time	<10 nsec
Fall time	<10 nsec
Propagation delay	0.1 μsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	0.45 mW at standby
	0.6 mW at 100 kHz
	1.8 mW at 1 MHz



CIRCUIT DIAGRAM 2 (Buffer-Driver)
MODULE #5811

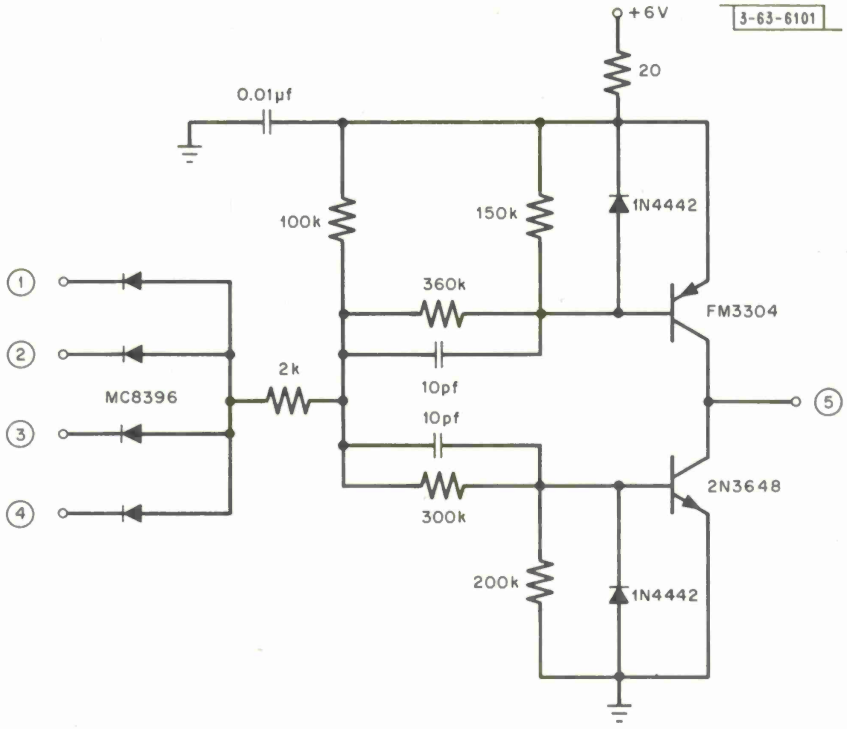


HORIZONTAL: 0.5 μsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 1 MHz

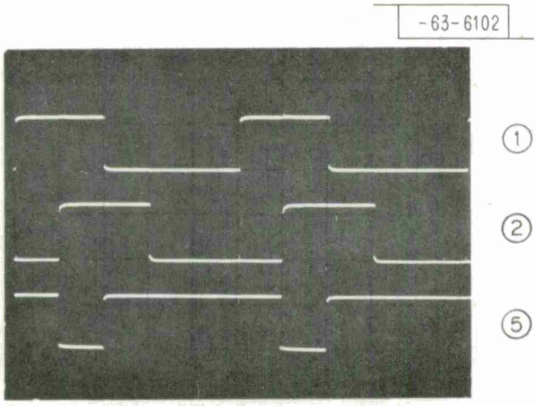
Circuit: Nand #5891

Operational Capabilities:	
Frequency range	0 to $\geqslant$1 MHz
Temperature range	$\geqslant \pm 50°C$
Supply voltage variation	$\geqslant \pm 25$ percent
Input Requirements:	
Maximum logic level degradation	$\geqslant \pm 10$ percent
Output Characteristics:	
Rise time	<10 nsec
Fall time	<10 nsec
Levels	≈ 0 and +6 volts
Other Characteristics:	
Power consumption	Input at +6 volts = 90 μW Input at ground = 360 μW Input at 100 kHz = 240 μW

#5891



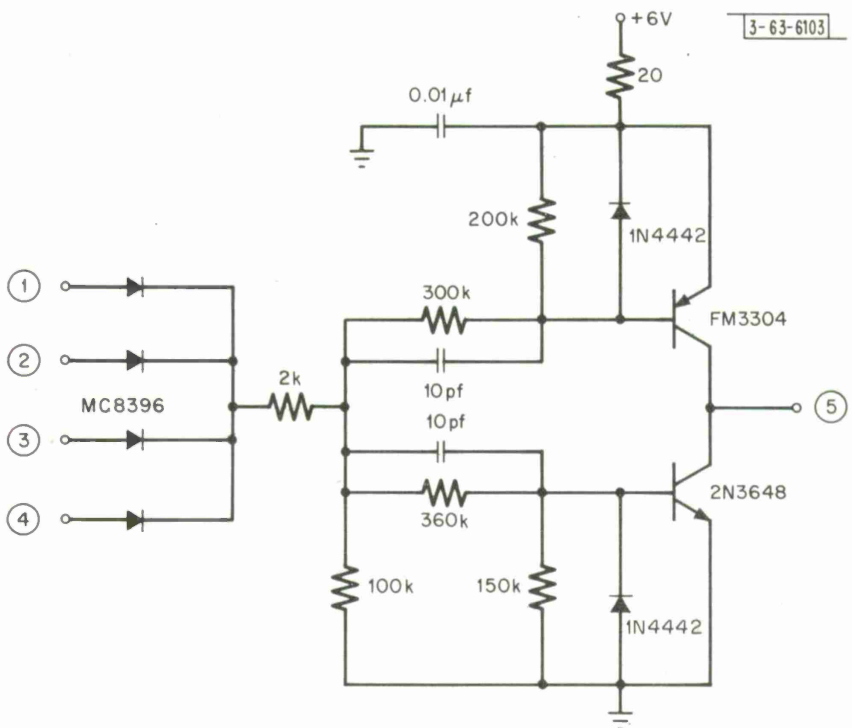
CIRCUIT DIAGRAM 3 (Nand)
MODULE #5891



HORIZONTAL: 2 µsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 100 kHz

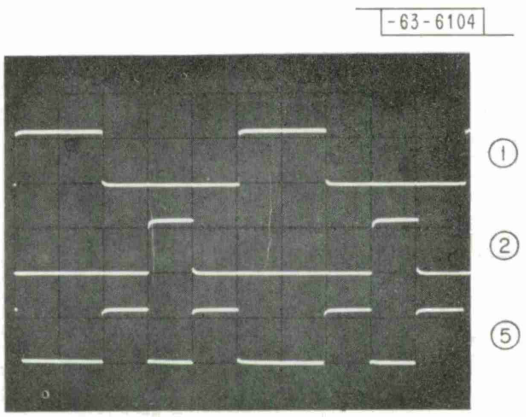
Circuit: Nor #5901

Operational Capabilities:	
Frequency range	0 to ⩾1 MHz
Temperature range	⩾±50°C
Supply voltage variation	⩾±25 percent
Input Requirements:	
Maximum logic level degradation	⩾±10 percent
Output Characteristics:	
Rise time	<10 nsec
Fall time	<10 nsec
Levels	≈0 and +6 volts
Other Characteristics:	
Power consumption	Input at +6 volts = 360 μW Input at ground = 90 μW 120 μW at 100 kHz = 12 μW



CIRCUIT DIAGRAM 4 (Nor)

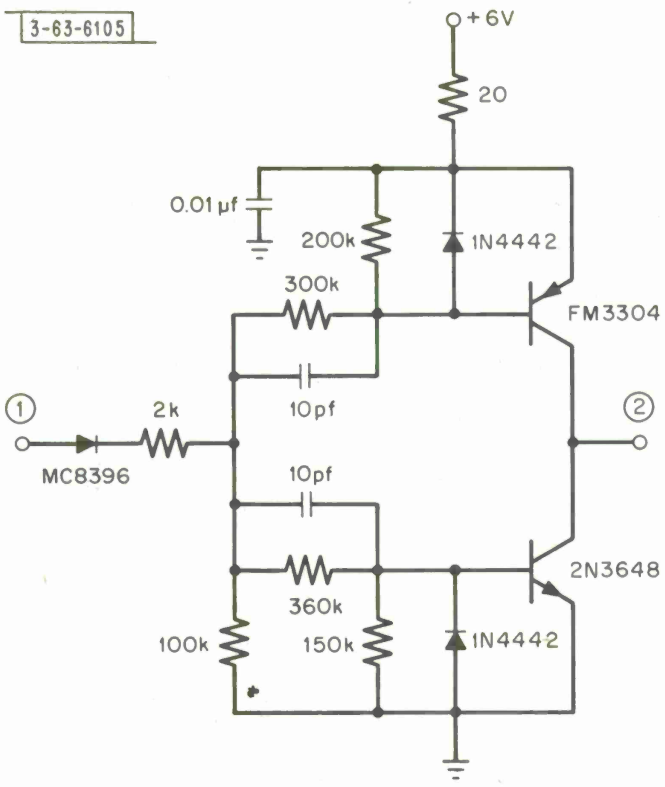
MODULE #5901



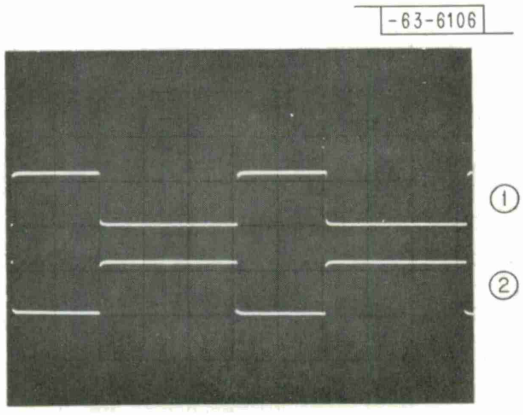
HORIZONTAL: 2μsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 100 kHz

Circuit: Inverter #5881

Operational Capabilities:	
Frequency range	0 to $\geqslant$1 MHz
Temperature range	$\geqslant \pm 50°C$
Supply voltage variation	$\geqslant \pm 25$ percent
Input Requirements:	
Maximum logic level degradation	$\geqslant \pm 10$ percent
Output Characteristics:	
Rise time	<10 nsec
Fall time	<10 nsec
Levels	≈ 0 and +6 volts
Other Characteristics:	
Power consumption	Input at +6 volts = 360 μW Input at ground = 90 μW Input at 100 kHz = 100 μW



CIRCUIT DIAGRAM 5 (Inverter)
MODULE #5881



HORIZONTAL: 2 µsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 100 kHz

III. LOW-, MEDIUM- AND HIGH-SPEED COMPLEMENTARY FLIP-FLOPS

Included in this section are various configurations of operational flip-flops. The circuit function, or combination of functions, provided by these configurations serves to fulfill most applications a flip-flop would be called upon to perform.

The complementary arrangement of transistors in the basic circuit has been used throughout because of the overall efficiency attained with this configuration.*

Circuit capabilities in all cases are stated and were arrived at through design refinements and compromises intended to place each configuration into a use category. Factors bringing about a need for compromise without detracting from a circuit's reliability in a given use category can be listed to include: commutating speed requirement, minimum standby power consumption, input sensitivity, noise immunity, maximum supply voltage variation, operational range vs temperature requirement, minimum component count, transistor economy, component size, and functional provisions such as set/reset.

All circuits have been modularized using discrete components and are standard equipment in ready-to-use form. For particular use requirements, these circuits are easily adaptable to modification and new module layout.

Because these circuits are intended for space system applications, much emphasis has been placed on minimal standby power relative to reliability. However, practices where power reductions would result at the expense of reliability have not been used.

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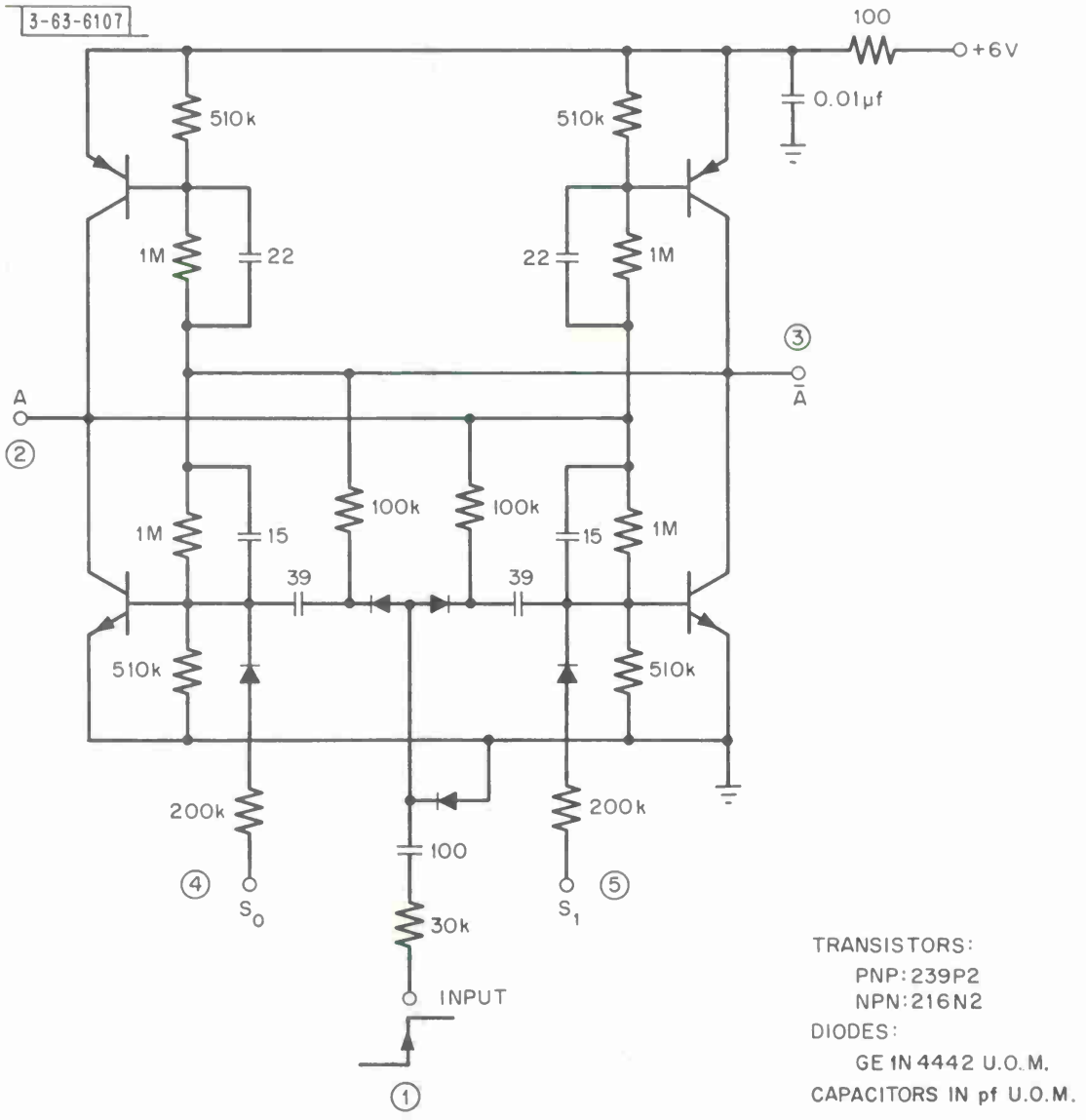
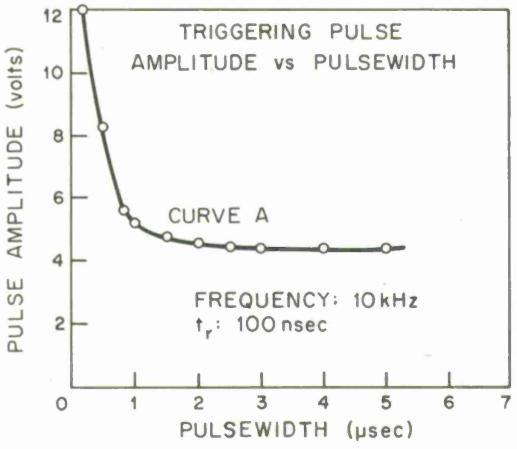
* R. H. Baker, "Maximum Efficiency Transistor Switching Circuits," Technical Report 110, Lincoln Laboratory, M.I.T. (22 March 1956), DDC 96497.

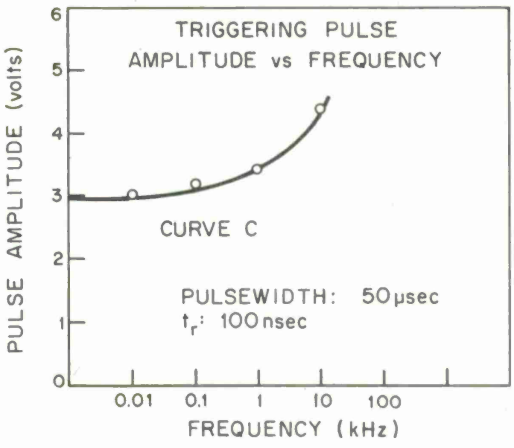
Circuit: Flip-Flop, Low-Frequency Counter-Storage #3481

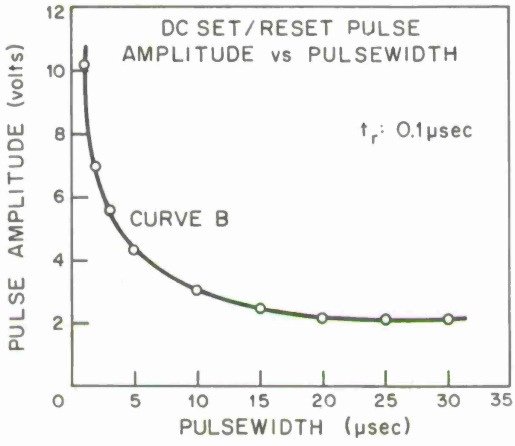
Operational Capabilities:	
Frequency range	0 to $\geqslant$10 kHz
Temperature range	$\geqslant \pm 50°C$
Supply voltage variation	$\geqslant \pm 30$ percent
Input Requirements:	
Trigger rise time	$\leqslant 2\,\mu$sec
Pulse amplitude	Curve A
Pulsewidth	Curve A
Set/reset	Curve B
Pulse amplitude with frequency	Curve C
Output Characteristics:	
Rise time	20 nsec
Fall time	30 nsec
Propagation delay	1.5 μsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	Standby = 60 μW
	10 kHz = 100 μW



CIRCUIT DIAGRAM 6 (Flip-Flop, Low-Frequency Counter-Storage)
MODULE # 3481







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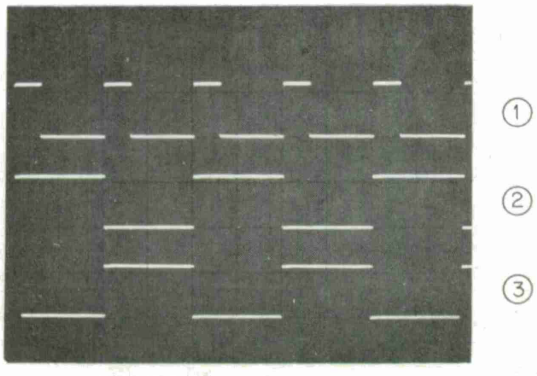
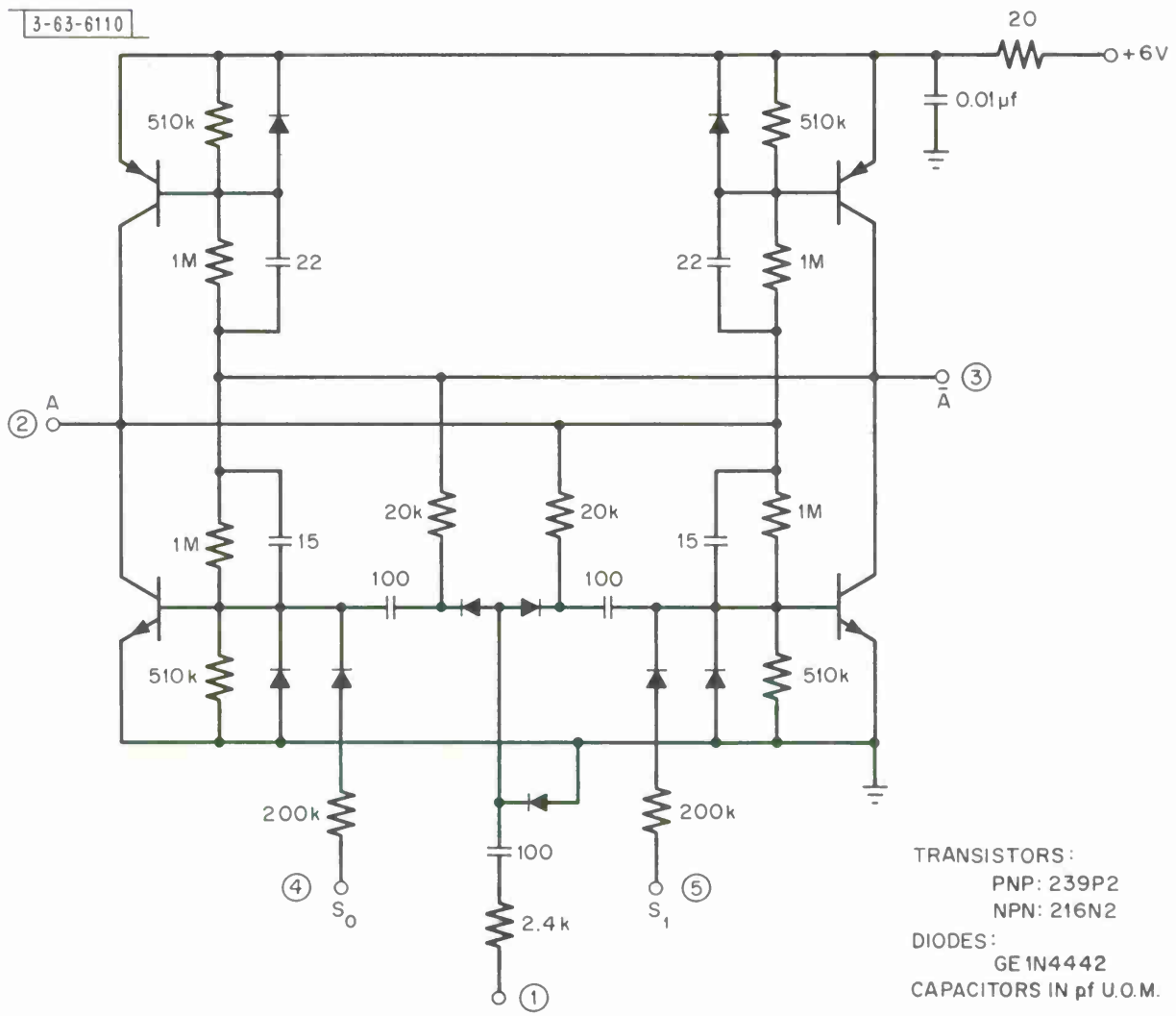
-63-6109



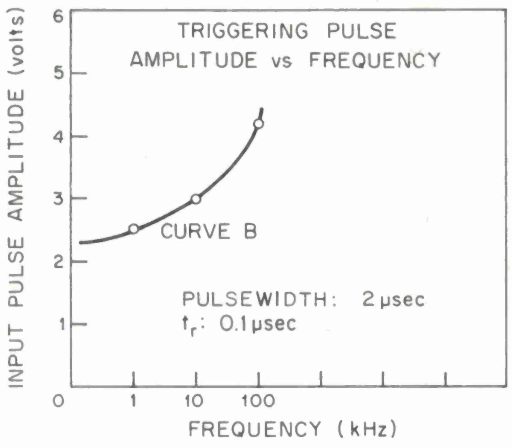
HORIZONTAL: 50 μsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 10 kHz

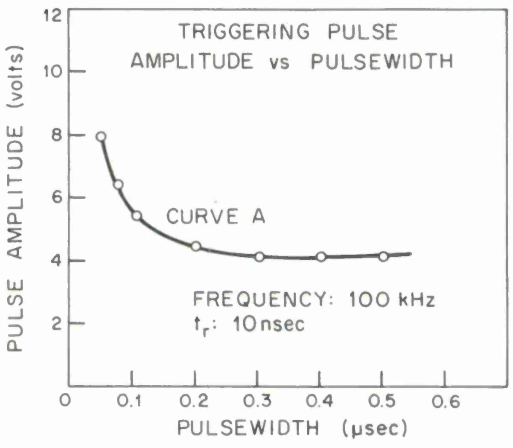
Circuit: Flip-Flop, Medium-Frequency Counter-Storage #3801

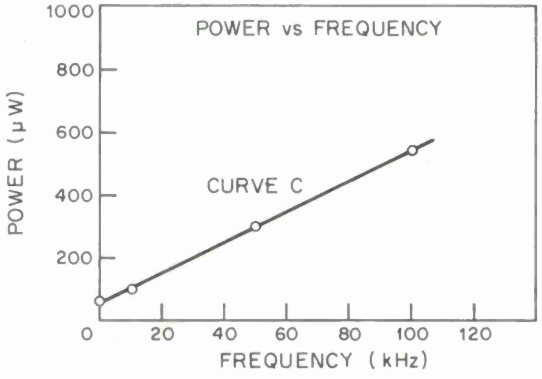
Operational Capabilities:	
Frequency range	0 to ≥100 kHz
Temperature range	≥±50°C
Supply voltage variation	≥±30 percent
Input Requirements:	
Trigger rise time	≤1 μsec
Pulse amplitude	Curve A
Pulsewidth	Curve A
Set/reset	#3481 curve B
Pulse amplitude with frequency	Curve B
Output Characteristics:	
Rise time	20 nsec
Fall time	50 nsec
Propagation delay	0.1 μsec
Levels	≈0 and +6 volts
Other Characteristics:	
Power consumption	Curve C



CIRCUIT DIAGRAM 7 (Flip-Flop, Medium-Frequency Counter-Storage)
MODULE # 3801







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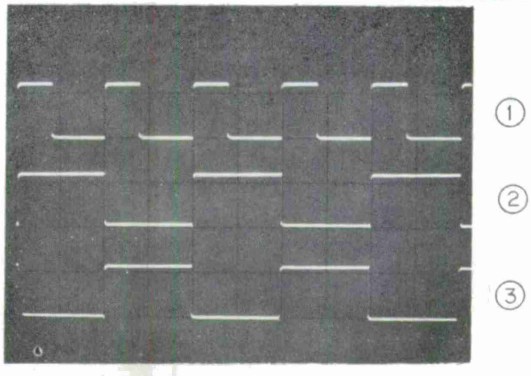
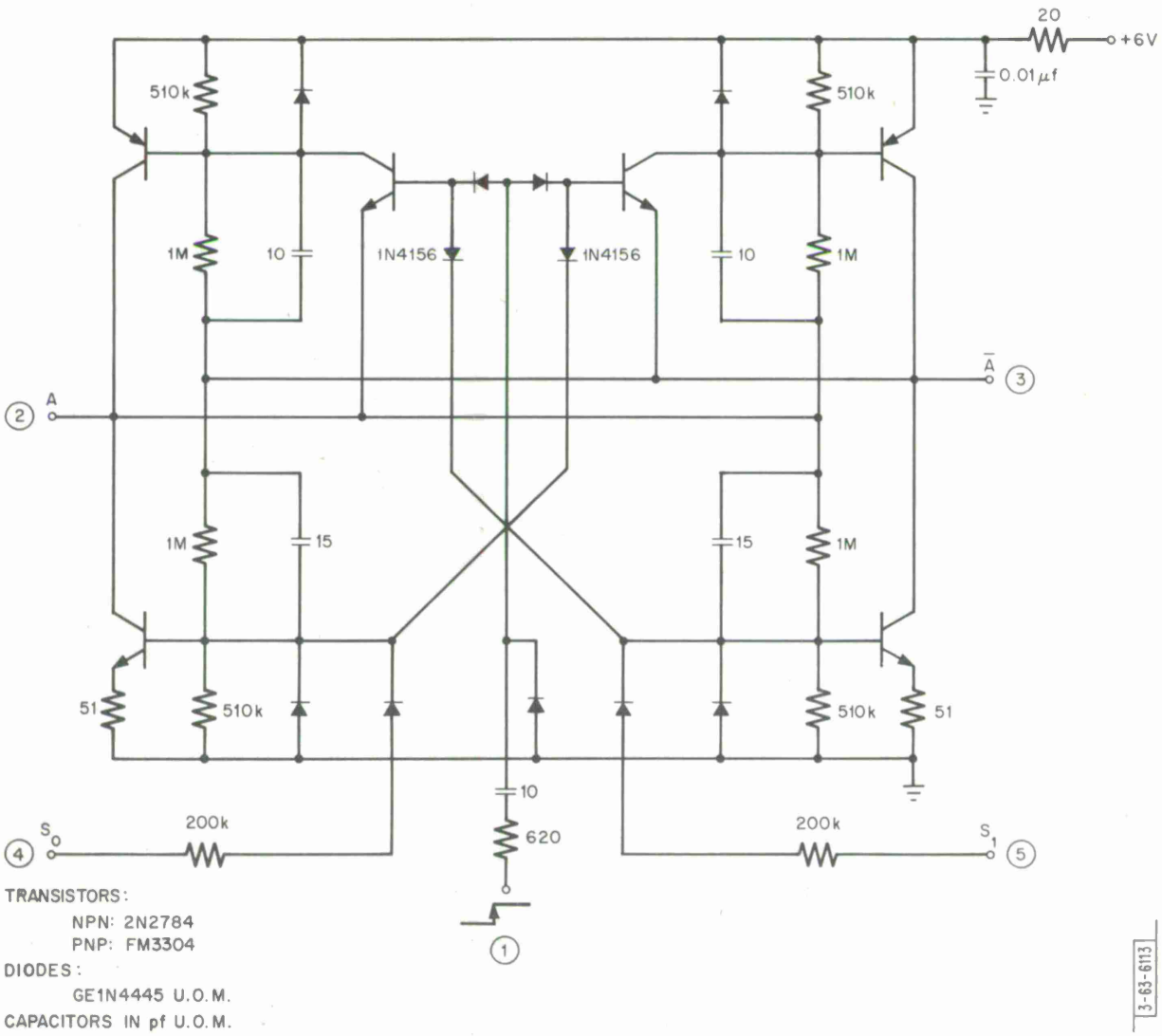
-63-6112



HORIZONTAL: 5 µsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 100 kHz

Circuit: Flip-Flop, High-Frequency Counter-Storage #3811

Operational Capabilities:	
Frequency range	0 to $\geq$1 MHz
Temperature range	$\geq \pm 50°C$
Supply voltage variation	$\geq \pm$ 30 percent
Input Requirements:	
Trigger rise time	$\leq$0.1 μsec
Pulse amplitude	Curve A
Pulsewidth	Curve A
Set/reset	Curve B
Output Characteristics:	
Rise time	$\leq$5 nsec
Fall time	$\leq$5 nsec
Propagation delay	$<$10 nsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	Curve C



TRANSISTORS:
NPN: 2N2784
PNP: FM3304
DIODES:
GE1N4445 U.O.M.
CAPACITORS IN pf U.O.M.

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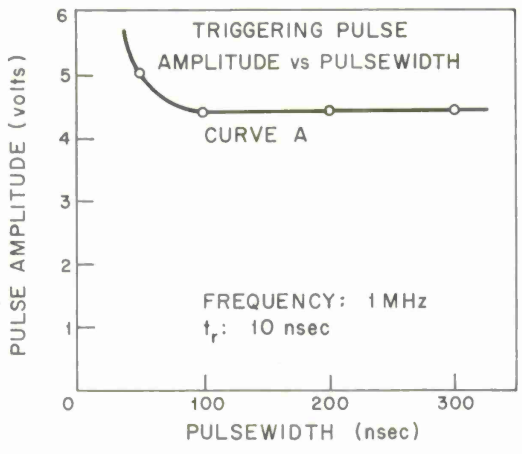
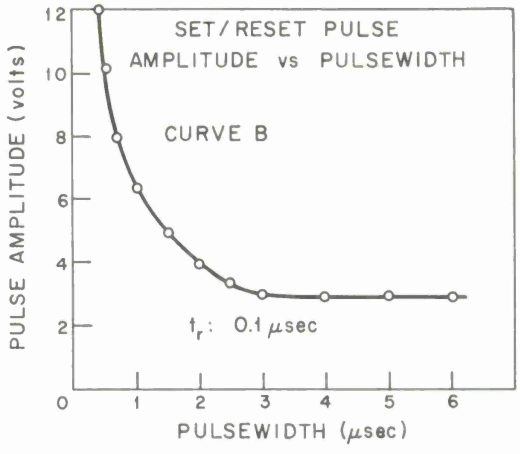
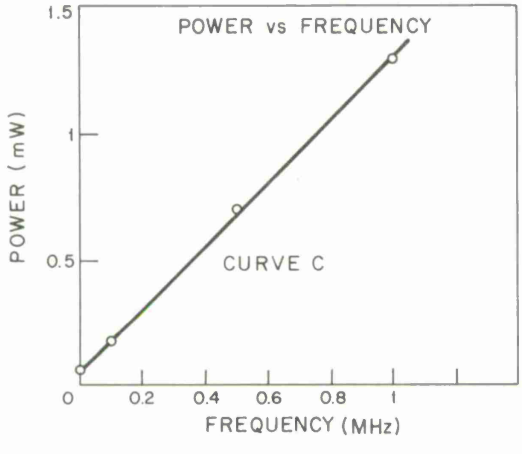
CIRCUIT DIAGRAM 8 (Flip-Flop, High-Frequency Counter-Storage)
MODULE # 3811

#3811







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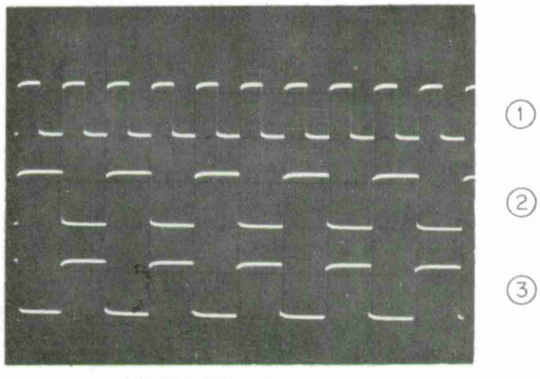
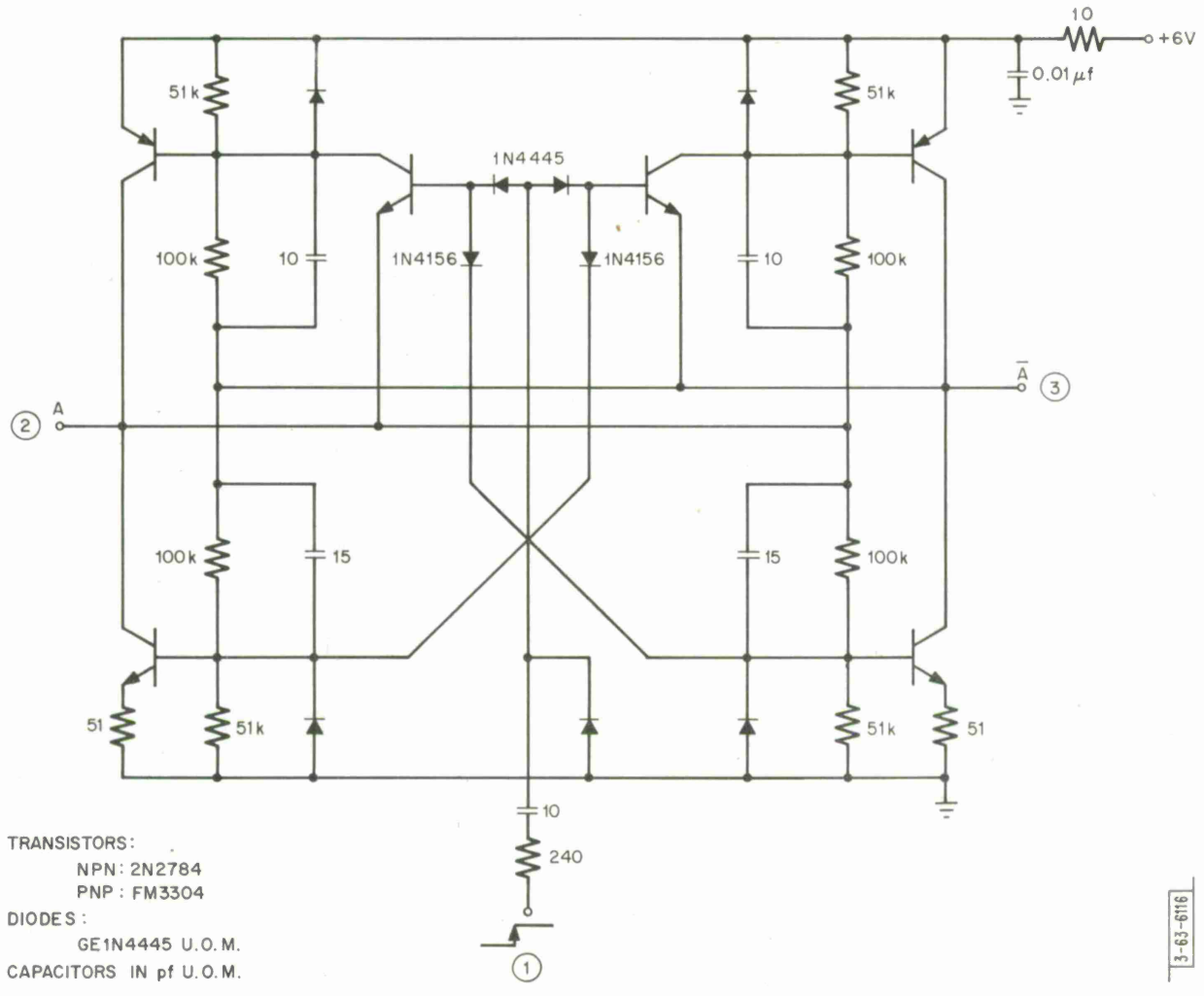


HORIZONTAL: 1 μsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 1 MHz

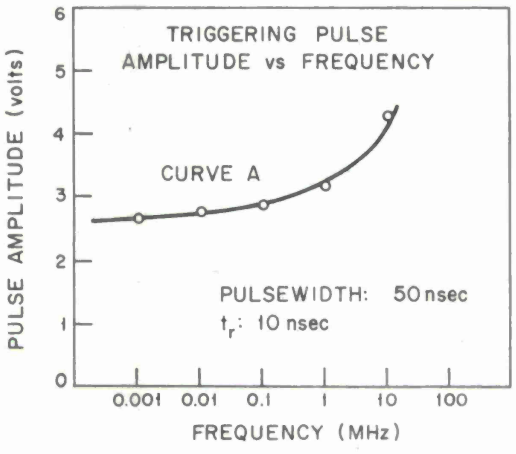
Circuit: Flip-Flop, Very High-Frequency Counter-Storage #3751

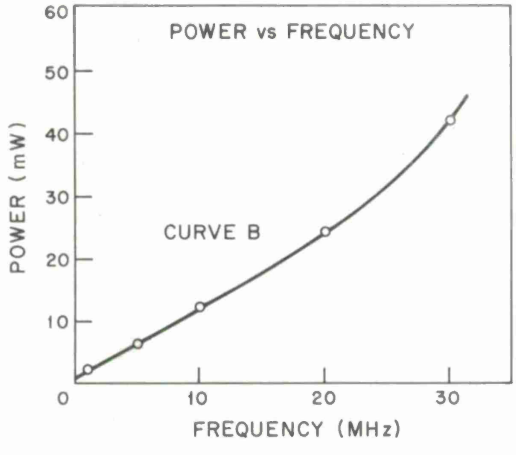
Operational Capabilities:	
Frequency range	0 to $\geqslant$30 MHz
Temperature range	$\geqslant \pm 50°C$
Supply voltage variation	$\geqslant \pm$ 25 percent
Input Requirements:	
Trigger rise time	$\leqslant$50 nsec
Pulse amplitude	6 volts ± 1 volt
Pulsewidth	$<$50 nsec
Pulse amplitude with frequency	Curve A
Output Characteristics:	
Rise time	$\leqslant$5 nsec
Fall time	$\leqslant$5 nsec
Propagation delay	$<$10 nsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	Curve B



CIRCUIT DIAGRAM 9 (Flip-Flop, Very High-Frequency Counter-Storage)
MODULE #3751

3-63-6117





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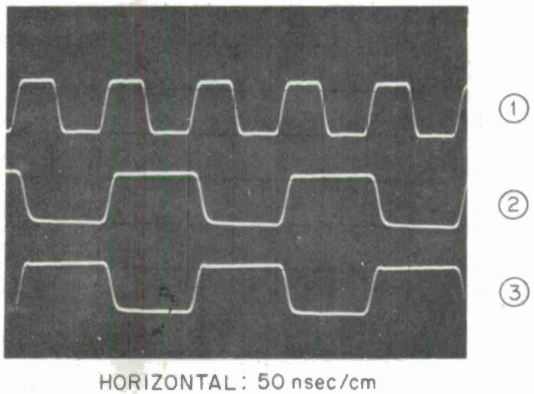
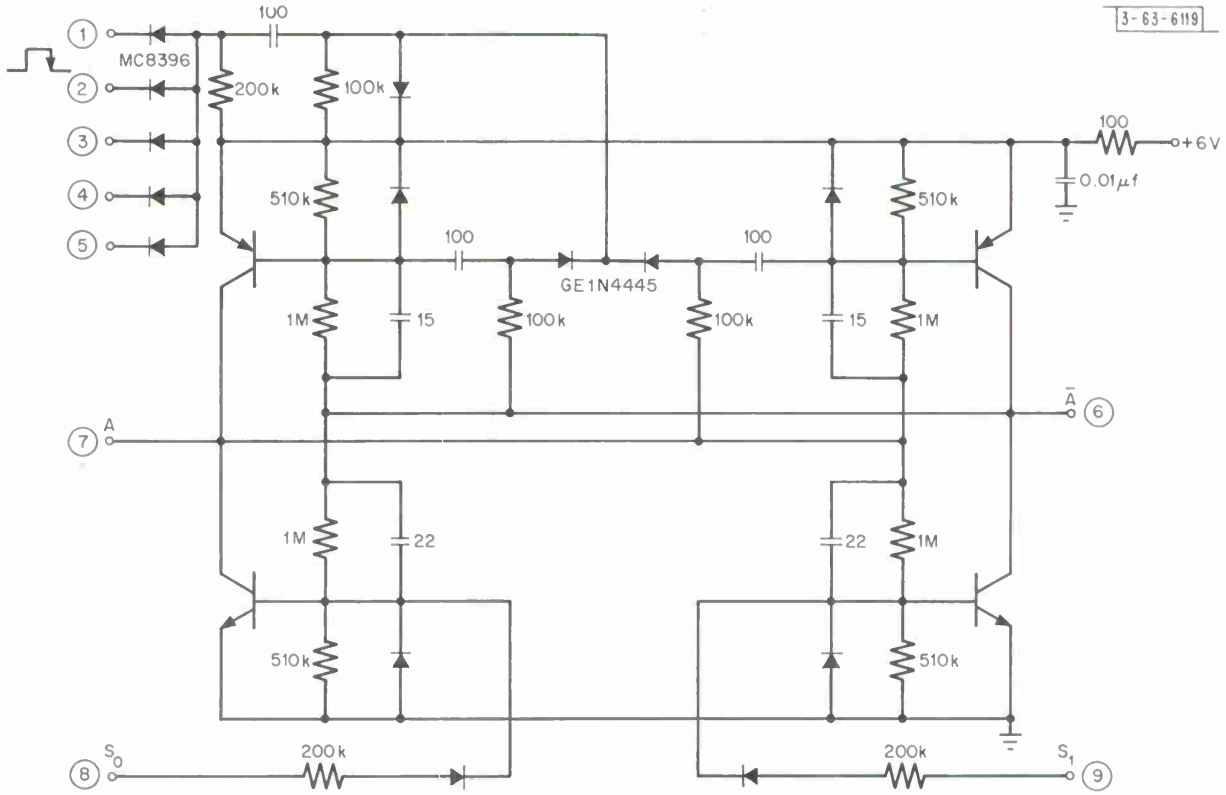


HORIZONTAL: 50 nsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 10 MHz

Circuit: Flip-Flop, Low-Frequency Parallel Counter #2831

Operational Capabilities:	
Frequency range	0 to ≥10 kHz
Temperature range	≥±50°C
Supply voltage variation	≥±20 percent
Input Requirements:	
Trigger fall time	≤2 μsec
Pulse amplitude	Curve A
Pulsewidth	Curve A
Set/reset	#3481 curve B
Pulse amplitude with frequency	Curve B
Output Characteristics:	
Rise time	30 nsec
Fall time	30 nsec
Propagation delay	40 nsec
Levels	≈0 and +6 volts
Other Characteristics:	
Power consumption	≈200 μW through 10 kHz

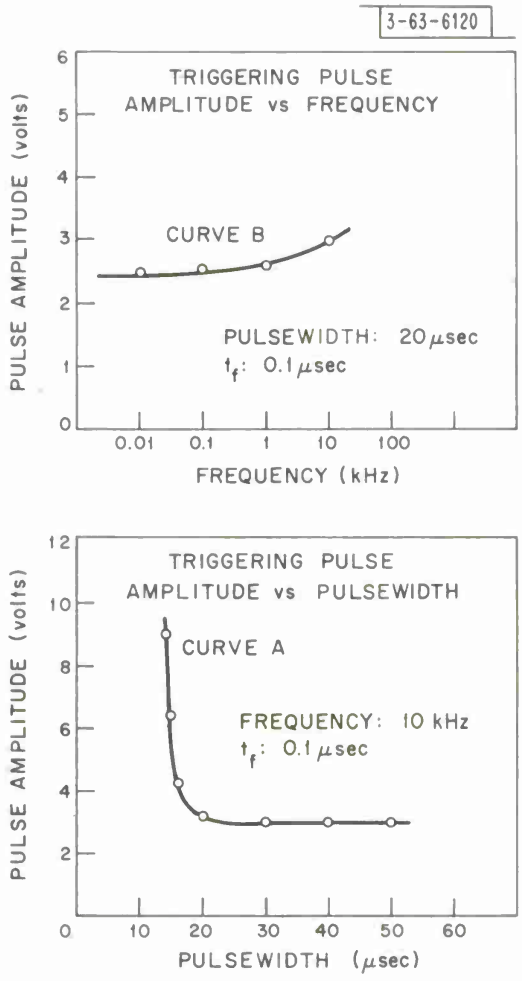


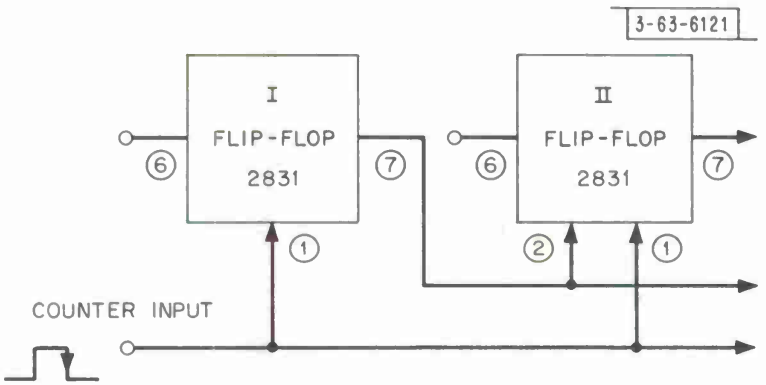
TRANSISTORS:
PNP: 239P2
NPN: 216N2

DIODES:
GE1N4442 U.O.M.

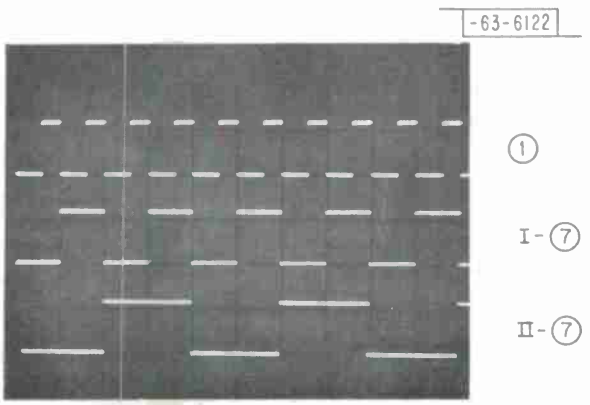
CAPACITORS IN pf U.O.M.

CIRCUIT DIAGRAM 10 (Flip-Flop, Low-Frequency Parallel Counter)
MODULE # 2831


3-63-6120
TRIGGERING PULSE
AMPLITUDE vs FREQUENCY
CURVE B
PULSEWIDTH: 20 μsec
t_f: 0.1 μsec
PULSE AMPLITUDE (volts)
FREQUENCY (kHz)
0.01
0.1
1
10
100
TRIGGERING PULSE
AMPLITUDE vs PULSEWIDTH
CURVE A
FREQUENCY: 10 kHz
t_f: 0.1 μsec
PULSE AMPLITUDE (volts)
PULSEWIDTH (μsec)



PARALLEL COUNTER APPLICATION

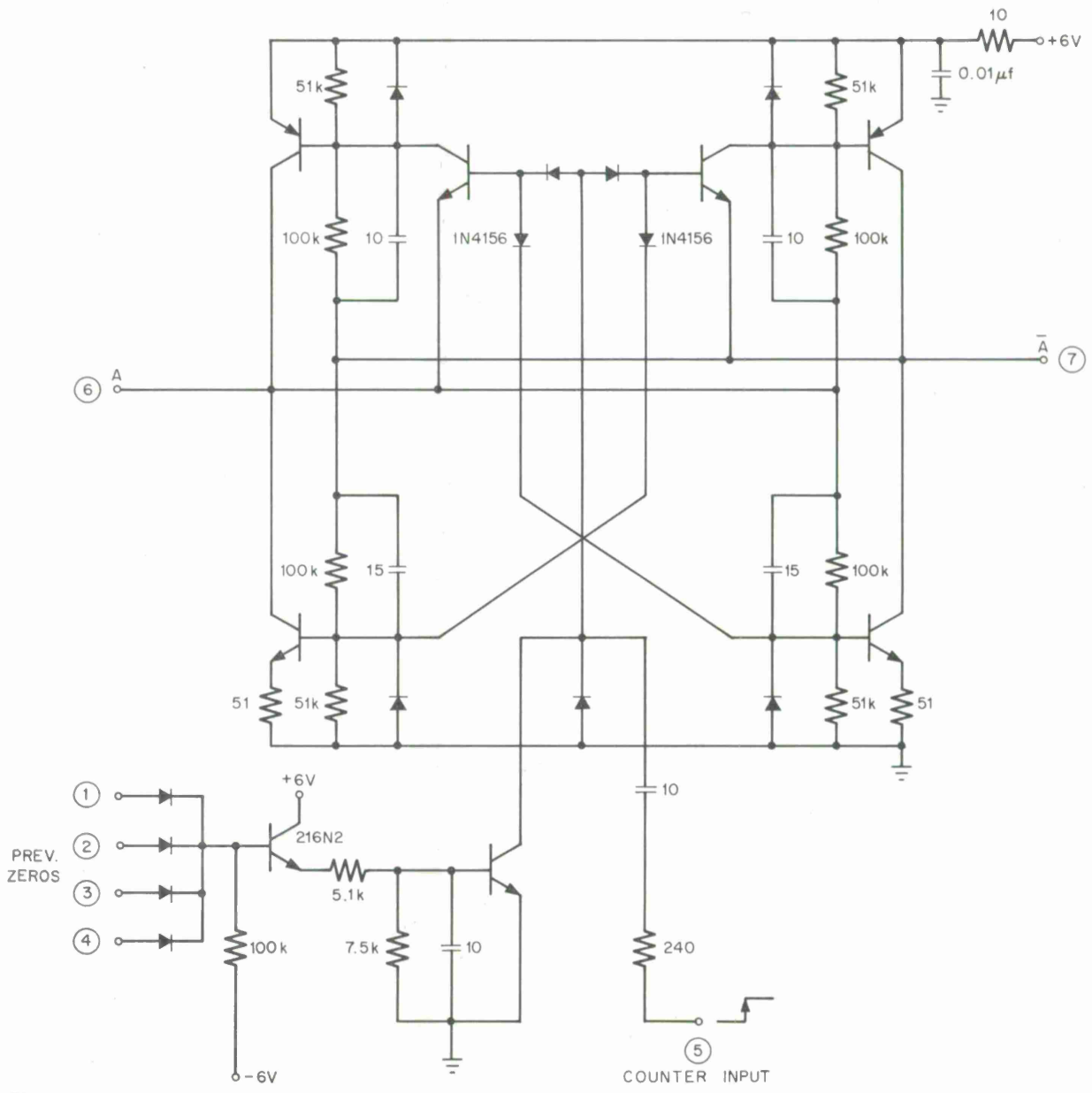


HORIZONTAL: 0.1 msec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 10 kHz

Circuit: Flip-Flop and Gate, High-Frequency Parallel Counter #5871

Operational Capabilities:	
Frequency range	0 to $\geqslant$20 MHz
Temperature range	$\geqslant \pm 50°C$
Supply voltage variation	$\geqslant \pm 20$ percent
Input Requirements:	
Trigger rise time	$\leqslant$50 nsec
Pulse amplitude	6 volts ± 1 volt
Pulsewidth	<50 nsec
Output Characteristics:	
Rise time	$\leqslant$5 nsec
Fall time	$\leqslant$5 nsec
Propagation delay	<10 nsec
Total 5-stage propagation delay	<10 nsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	+6 volts (see curve A) −6 volts = −0.5 mW

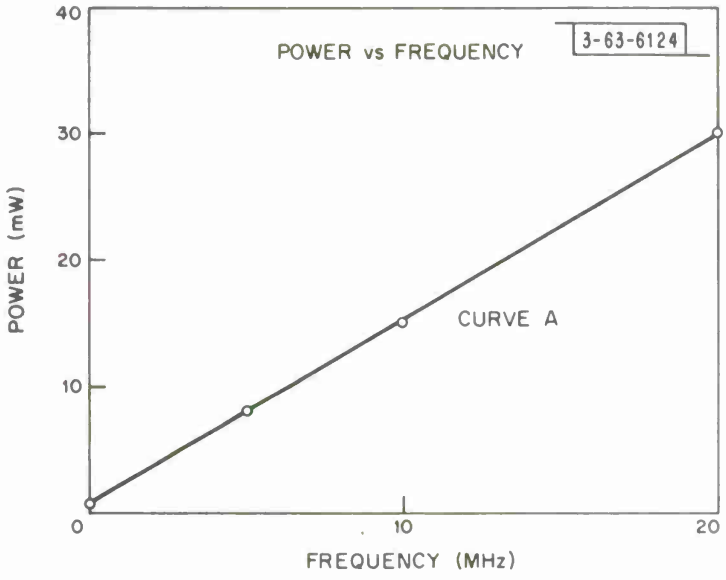
#5871

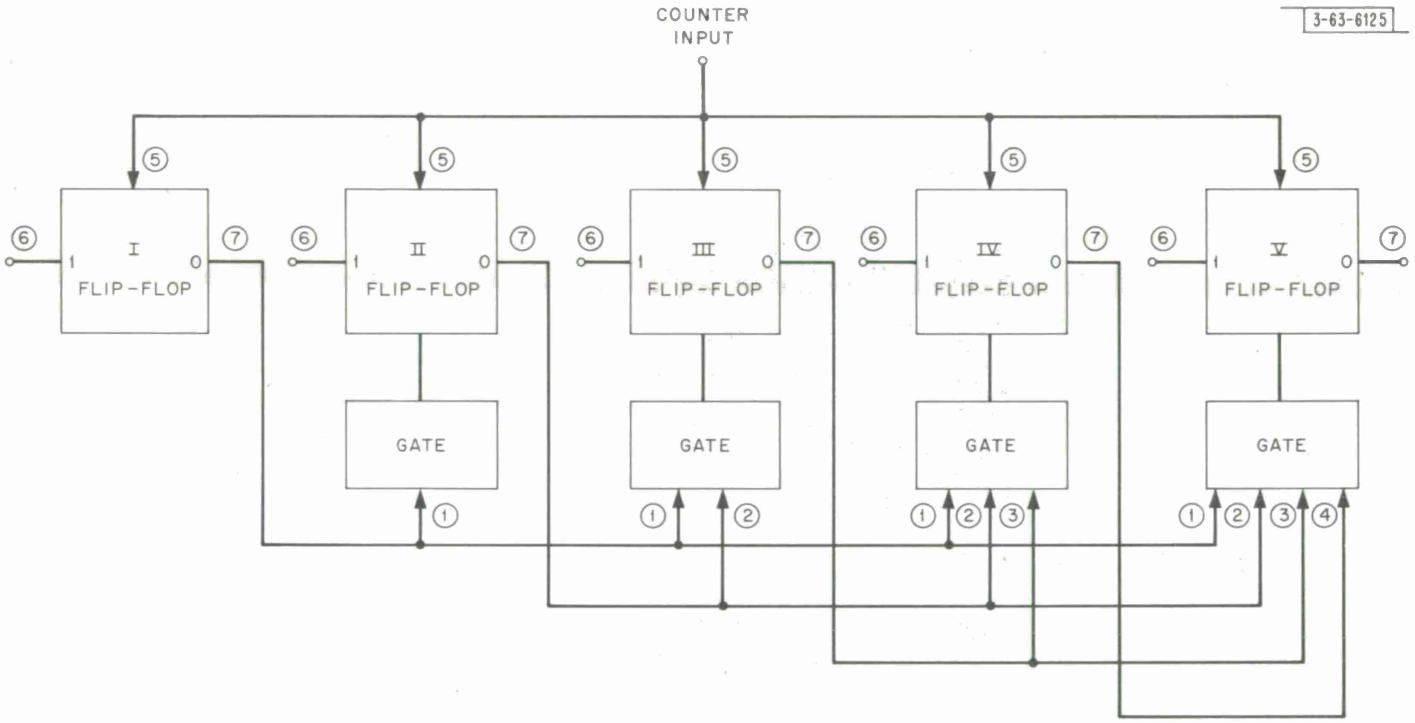


TRANSISTORS:
NPN: 2N2784
PNP: FM3304
DIODES:
GE1N4445 U.O.M.
CAPACITORS IN pf U.O.M.

3-63-6123

CIRCUIT DIAGRAM 11 (Flip-Flop and Gate, High-Frequency Parallel Counter)
MODULE #5871

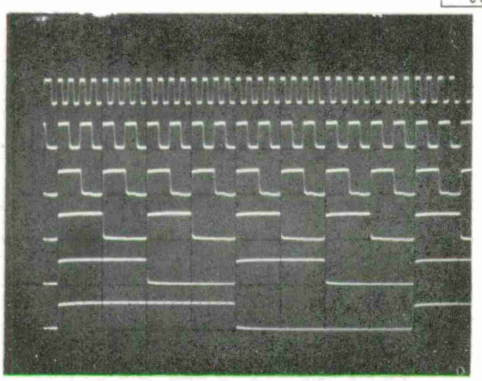

POWER vs FREQUENCY
3-63-6124
40
30
20
10
0
10
20
POWER (mW)
FREQUENCY (MHz)
CURVE A



FIVE-STAGE, HIGH-SPEED, PARALLEL COUNTER TEST APPLICATION

#5871

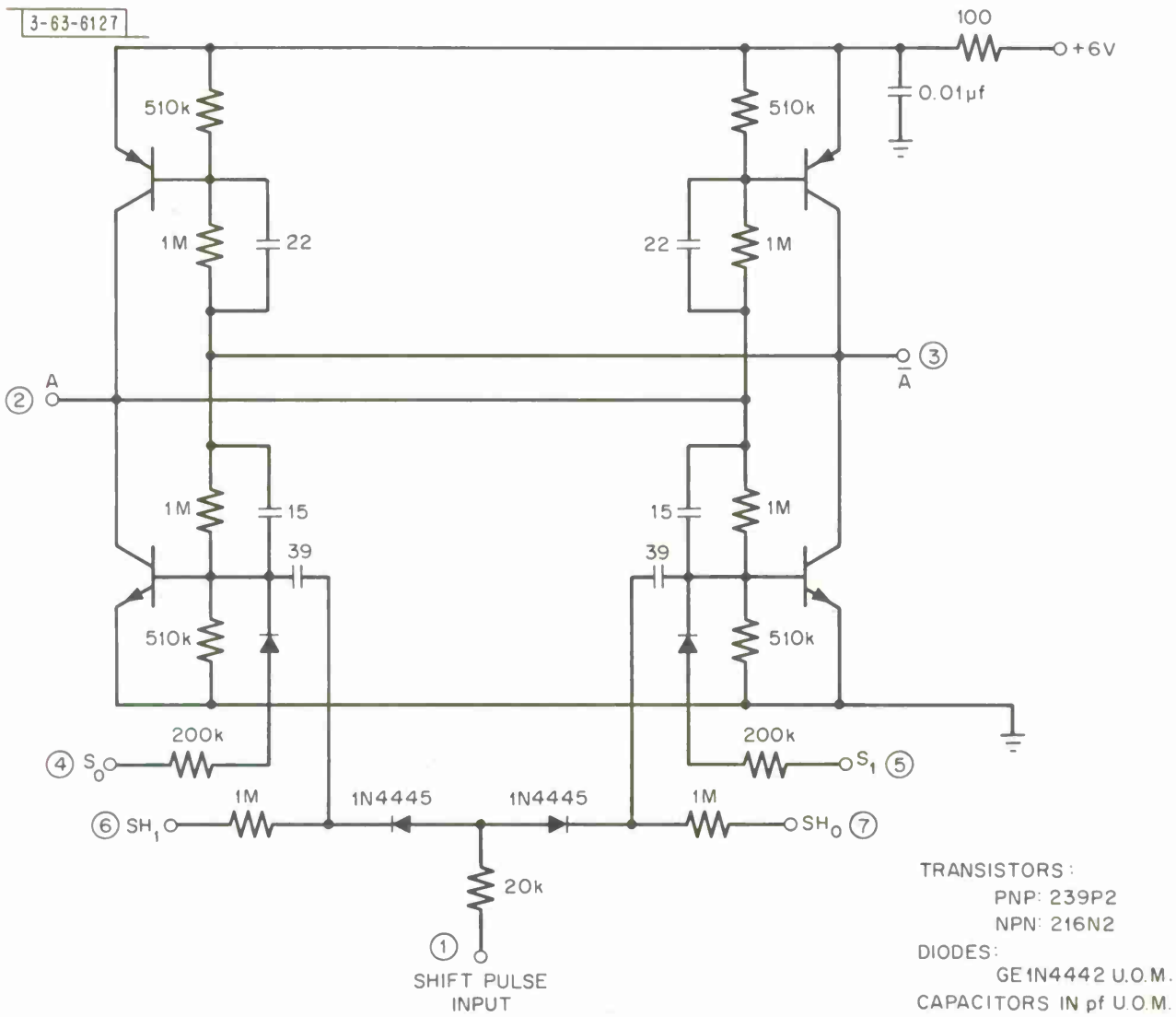
-63-6126



HORIZONTAL: 0.5 μsec/cm
VERTICAL: 10 V/cm
WAVEFORMS AT ≈10 MHz

Circuit: Flip-Flop, Low-Frequency Shift Register #3791

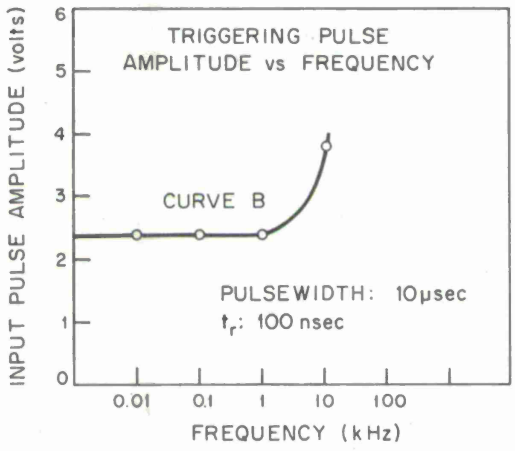
Operational Capabilities:	
Frequency range	0 to $\geq$10 kHz
Temperature range	$\geq \pm 50°C$
Supply voltage variation	$\geq \pm 20$ percent
Input Requirements:	
Trigger rise time	$\leq 10\,\mu$sec
Pulse amplitude	Curve A
Pulsewidth	Curve A
Set/reset	#3481 curve B
Pulse amplitude with frequency	Curve B
Output Characteristics:	
Rise time	20 nsec
Fall time	30 nsec
Propagation delay	0.5 μsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	Standby = 60 μW
	10 kHz = 100 μW

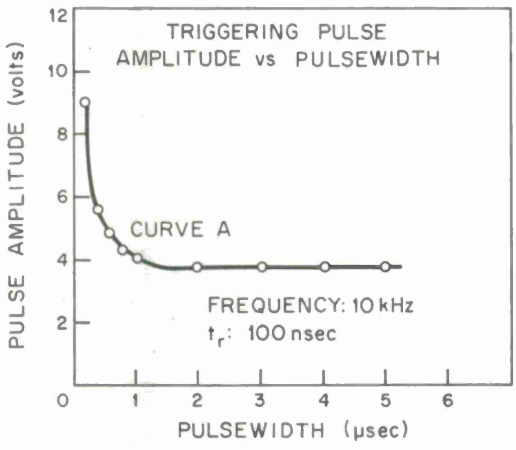


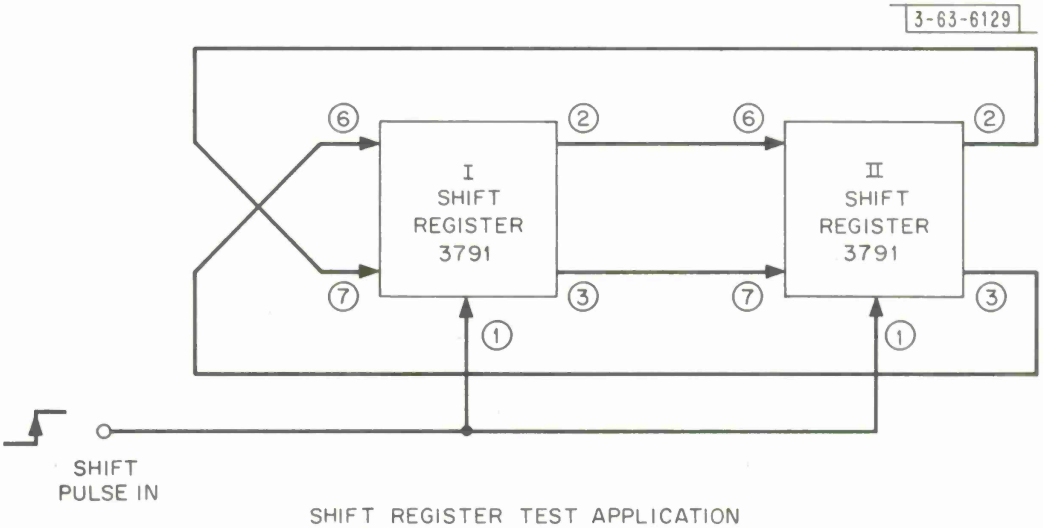
CIRCUIT DIAGRAM 12 (Flip-Flop, Low-Frequency Shift Register)
MODULE # 3791

#3791

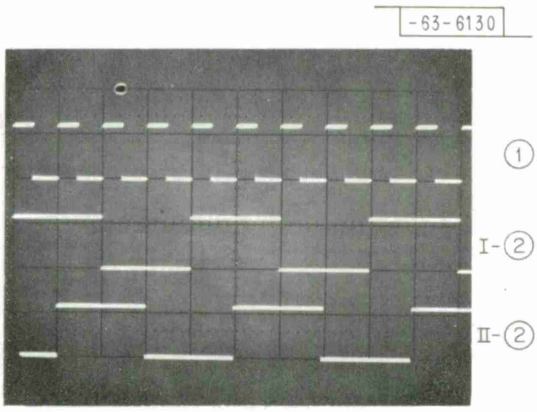
3-63-6128







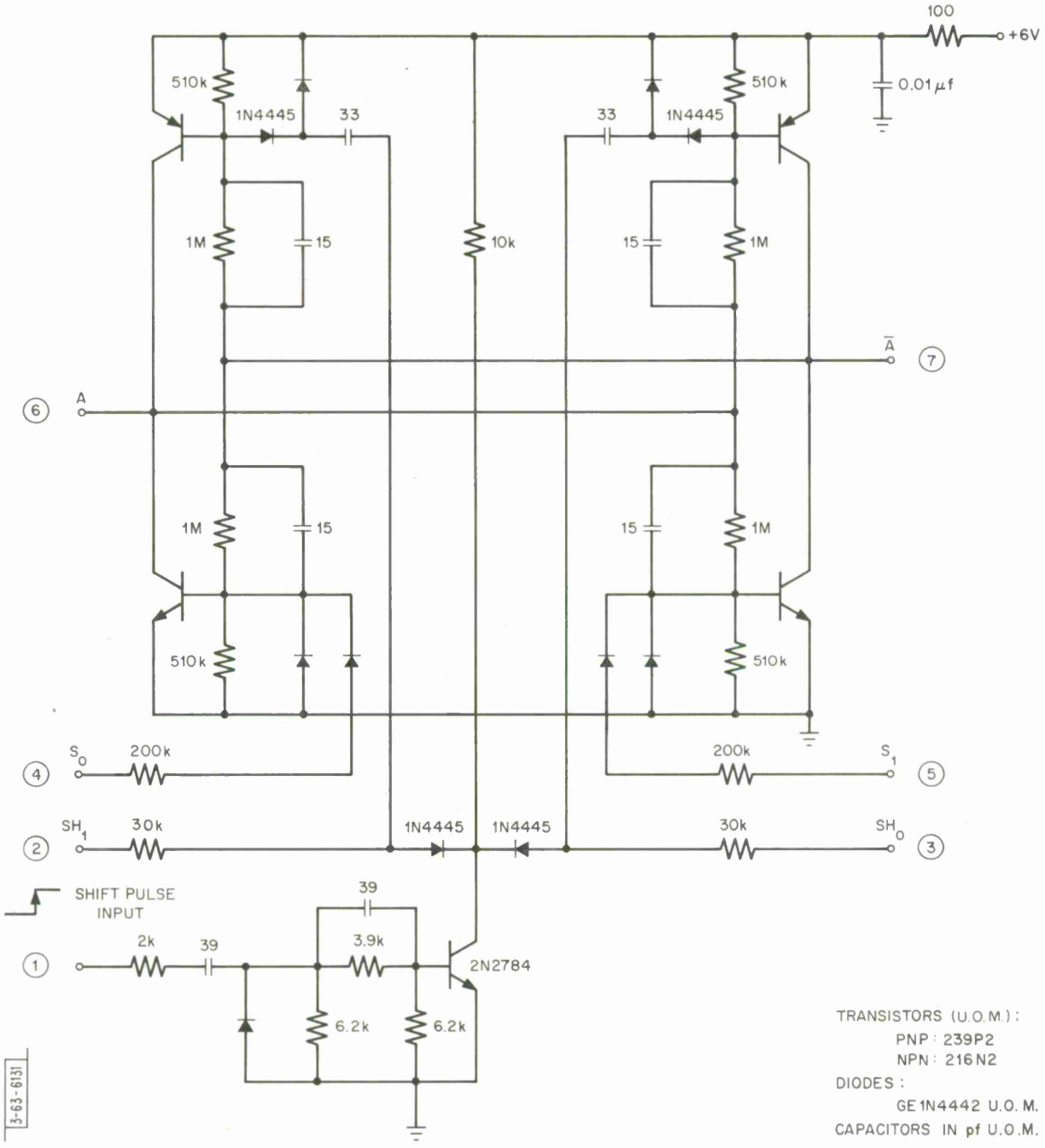
SHIFT REGISTER TEST APPLICATION



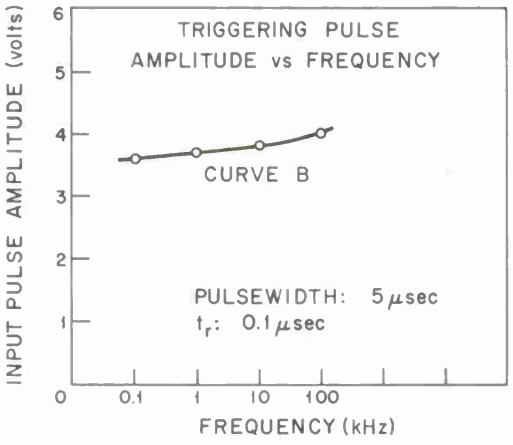
HORIZONTAL: 0.1msec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 10 kHz

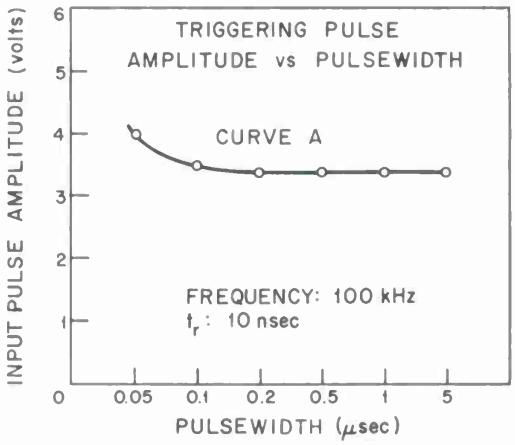
Circuit: Flip-Flop, Medium-Frequency Shift Register #3571-1

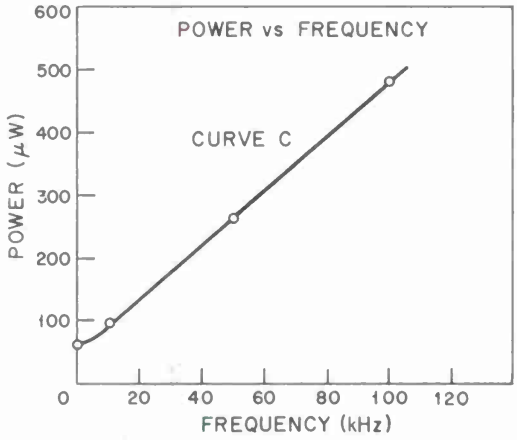
Operational Capabilities:	
Frequency range	0 to $\geq$100 kHz
Temperature range	$\geq \pm 50°C$
Supply voltage variation	$\geq \pm 20$ percent
Input Requirements:	
Trigger rise time	≤ 0.2 μsec
Pulse amplitude	Curve A
Pulsewidth	Curve A
Set/reset	#3481 curve B
Pulse amplitude with frequency	Curve B
Output Characteristics:	
Rise time	25 nsec
Fall time	30 nsec
Propagation delay	40 nsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	Curve C



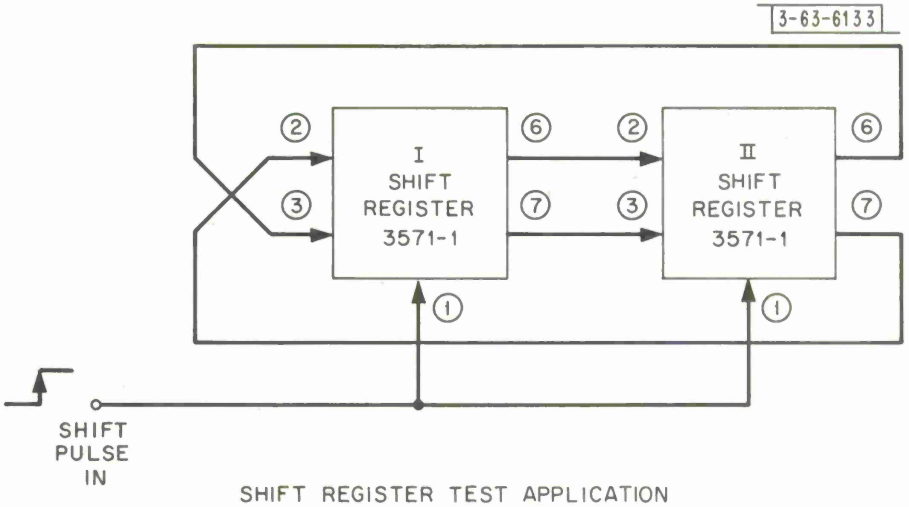
CIRCUIT DIAGRAM 13 (Flip-Flop, Medium-Frequency Shift Register)
MODULE # 3571-1


TRIGGERING PULSE
AMPLITUDE vs FREQUENCY
CURVE B
PULSEWIDTH: 5 μsec
t_r: 0.1 μsec
INPUT PULSE AMPLITUDE (volts)
FREQUENCY (kHz)
0
1
2
3
4
5
6
0.1
1
10
100

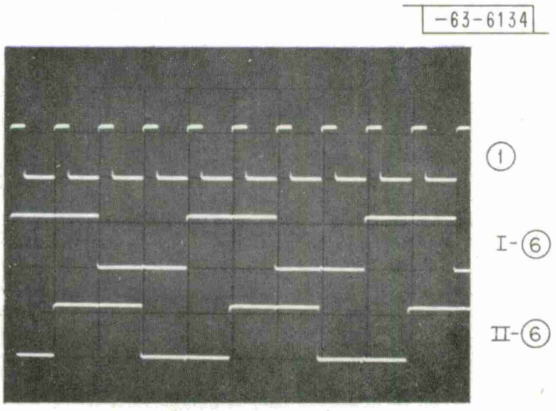

TRIGGERING PULSE
AMPLITUDE vs PULSEWIDTH
CURVE A
FREQUENCY: 100 kHz
t_r: 10 nsec
INPUT PULSE AMPLITUDE (volts)
PULSEWIDTH (μsec)
0
1
2
3
4
5
6
0.05
0.1
0.2
0.5
1
5


POWER vs FREQUENCY
CURVE C
POWER (μW)
FREQUENCY (kHz)
0
100
200
300
400
500
600
20
40
60
80
100
120

3-63-6132



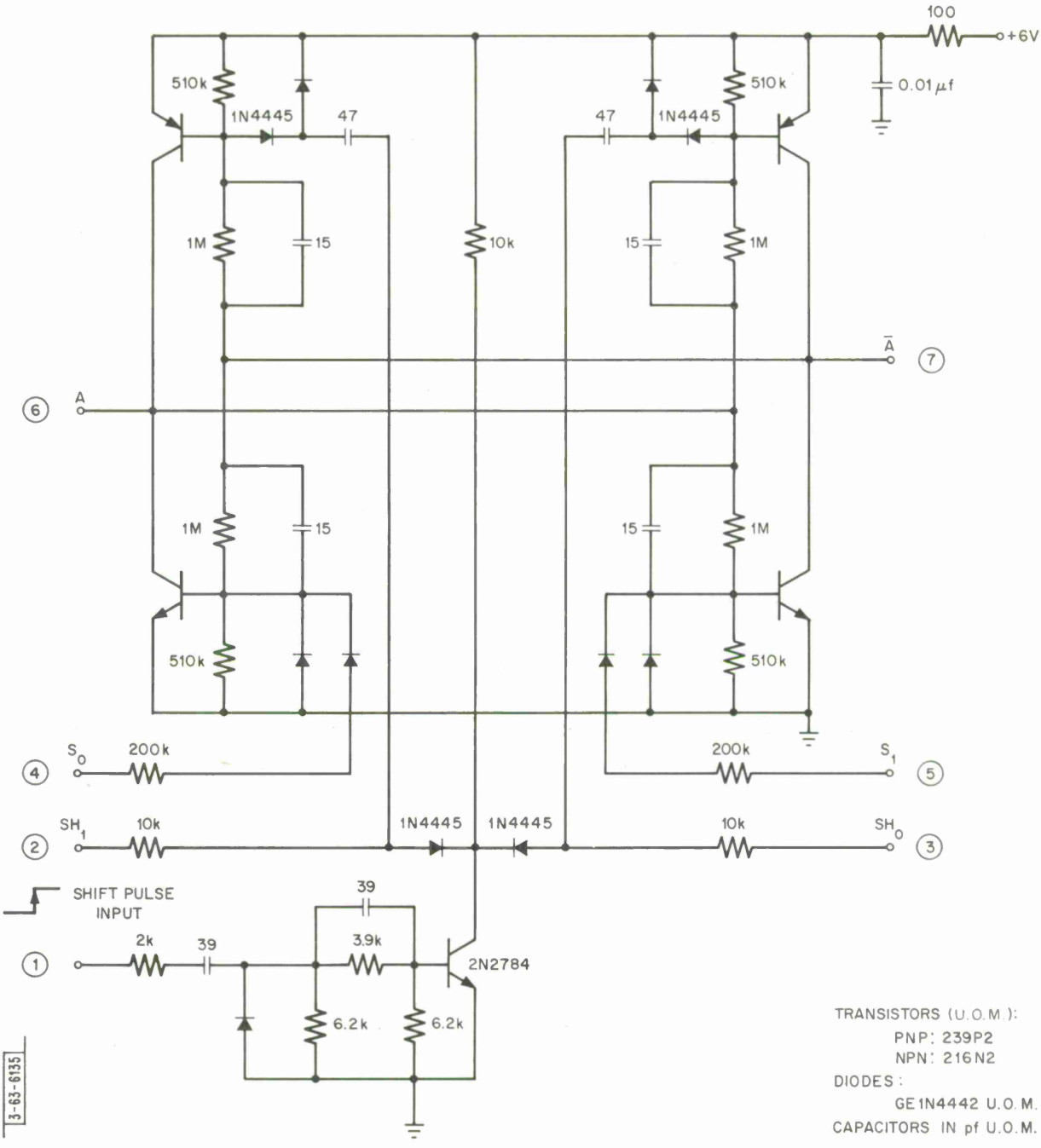
SHIFT REGISTER TEST APPLICATION



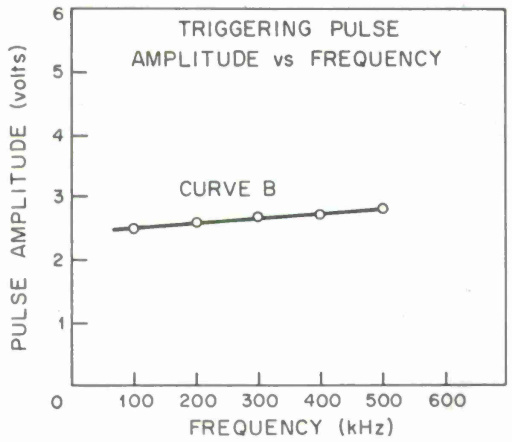
HORIZONTAL: 10 μsec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 100 kHz

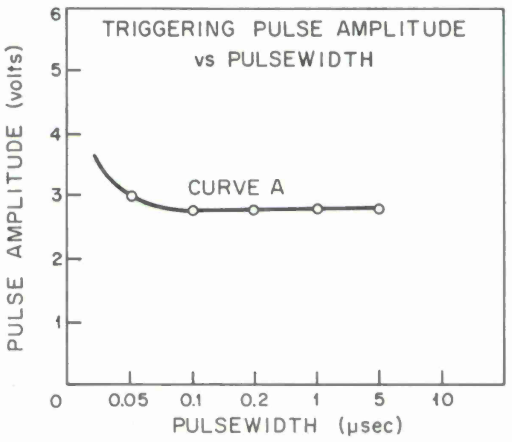
Circuit: Flip-Flop, High-Frequency Shift Register #3571-2

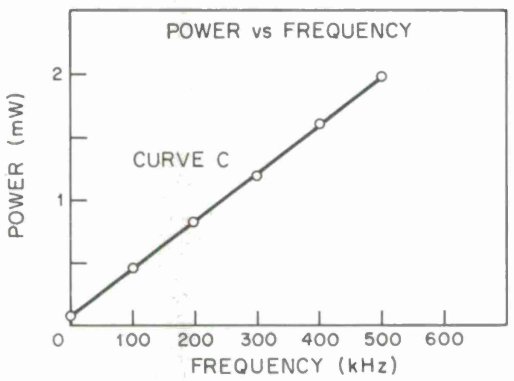
Operational Capabilities:	
Frequency range	0 to $\geqslant$500 kHz
Temperature range	$\geqslant\pm$50°C
Supply voltage variation	$\geqslant\pm$20 percent
Input Requirements:	
Trigger rise time	$\leqslant$0.2 μsec
Pulse amplitude	Curve A
Pulsewidth	Curve A
Set/reset	#3481 curve B
Pulse amplitude with frequency	Curve B
Output Characteristics:	
Rise time	20 nsec
Fall time	25 nsec
Propagation delay	30 nsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	Curve C



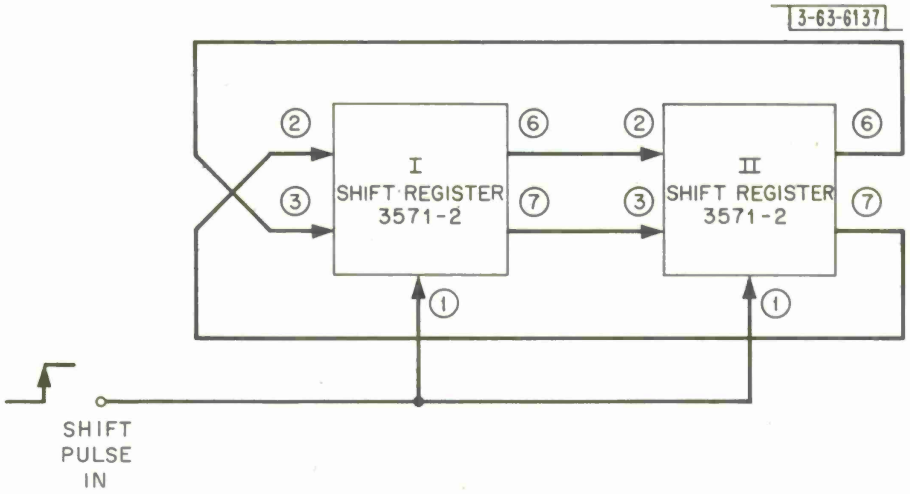
CIRCUIT DIAGRAM 14 (Flip-Flop, High-Frequency Shift Register)
MODULE # 3571-2


TRIGGERING PULSE
AMPLITUDE vs FREQUENCY
CURVE B
PULSE AMPLITUDE (volts)
0
1
2
3
4
5
6
100
200
300
400
500
600
FREQUENCY (kHz)

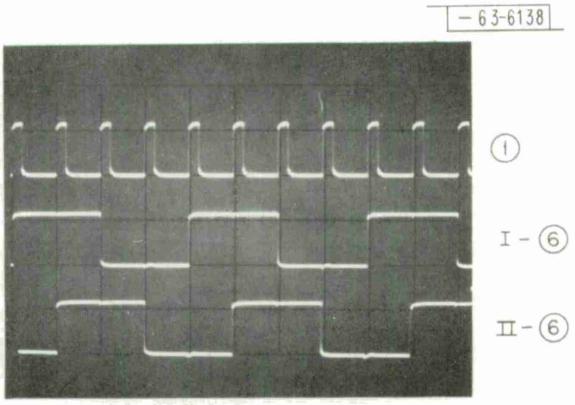

TRIGGERING PULSE AMPLITUDE
vs PULSEWIDTH
CURVE A
PULSE AMPLITUDE (volts)
0
1
2
3
4
5
6
0.05
0.1
0.2
1
5
10
PULSEWIDTH (μsec)


POWER vs FREQUENCY
CURVE C
POWER (mW)
0
1
2
100
200
300
400
500
600
FREQUENCY (kHz)

3-63-6136



SHIFT REGISTER TEST APPLICATION



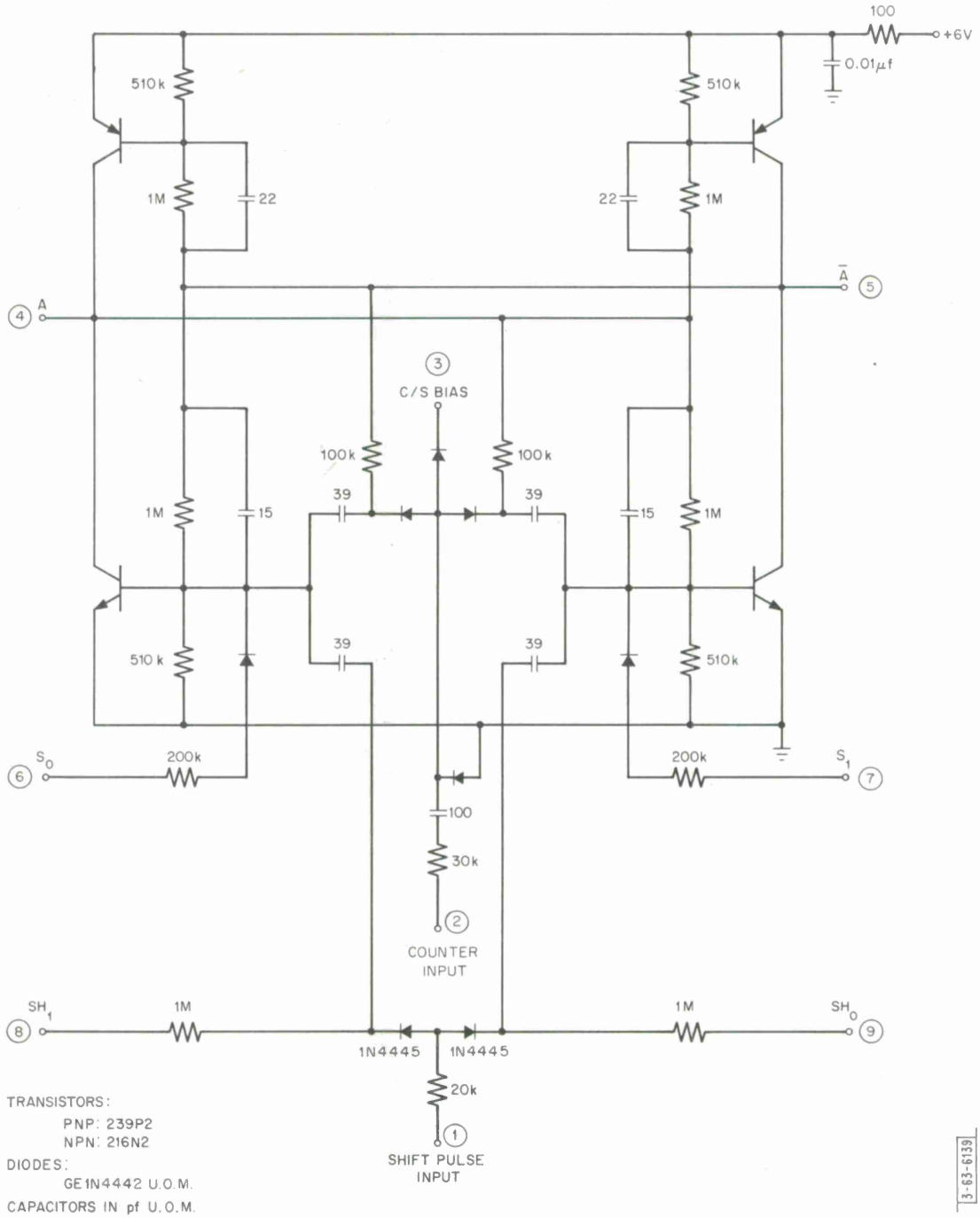
HORIZONTAL: 2 μsec/cm
VERTICAL: 5 V/cm

Circuit: Flip-Flop, Low-Frequency Counter/Shift Register (Counter Section) #3491

Operational Capabilities:	
Frequency range	0 to $\geqslant$10 kHz
Temperature range	$\geqslant \pm 50°C$
Supply voltage variation	$\geqslant \pm 20$ percent
Input Requirements:	
Trigger rise time	$\leqslant 2\,\mu$sec
Pulse amplitude	Curve A
Pulsewidth	Curve A
Set/reset	#3481 curve B
Pulse amplitude with frequency	Curve B
Output Characteristics:	
Rise time	20 nsec
Fall time	30 nsec
Propagation delay	1.5 μsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	Standby = 60 μW
	10 kHz = 100 μW

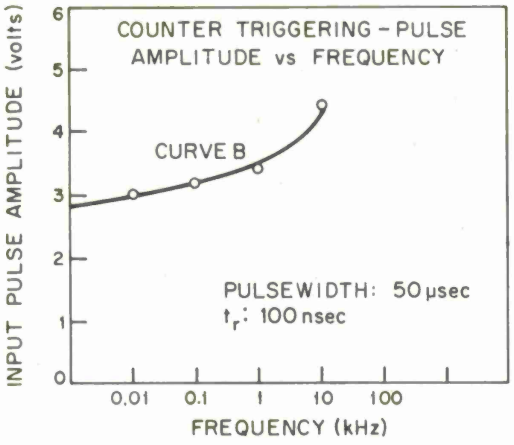
Circuit: Flip-Flop, Low-Frequency Counter/Shift Register (Shift Register Section) #3491

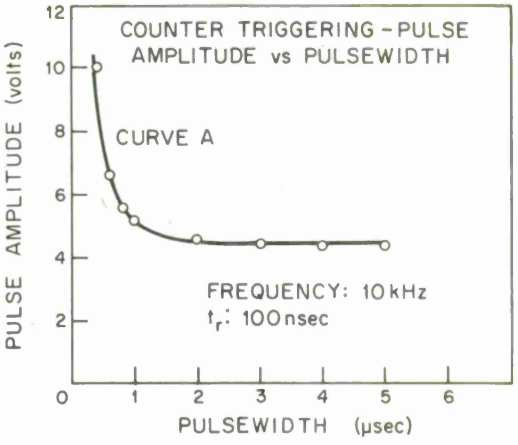
Operational Capabilities:	
Frequency range	0 to ≥10 kHz
Temperature range	≥±50°C
Supply voltage variation	≥±20 percent
Input Requirements:	
Trigger rise time	≤5 μsec
Pulse amplitude	Curve C
Pulsewidth	Curve C
Set/reset	#3481 curve B
Pulse amplitude with frequency	Curve D
Output Characteristics:	
Rise time	20 nsec
Fall time	30 nsec
Propagation delay	0.5 μsec
Levels	≈0 and +6 volts
Other Characteristics:	
Power consumption	Standby = 60 μW
	10 kHz = 100 μW

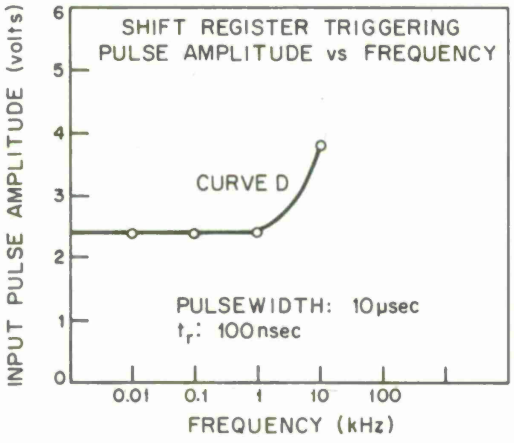


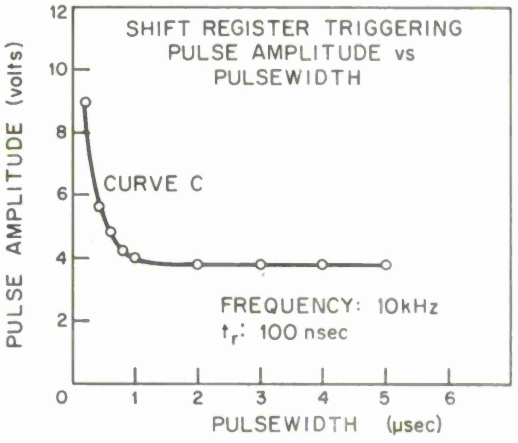
CIRCUIT DIAGRAM 15 (Flip-Flop, Low-Frequency Counter/Shift Register)
MODULE # 3491

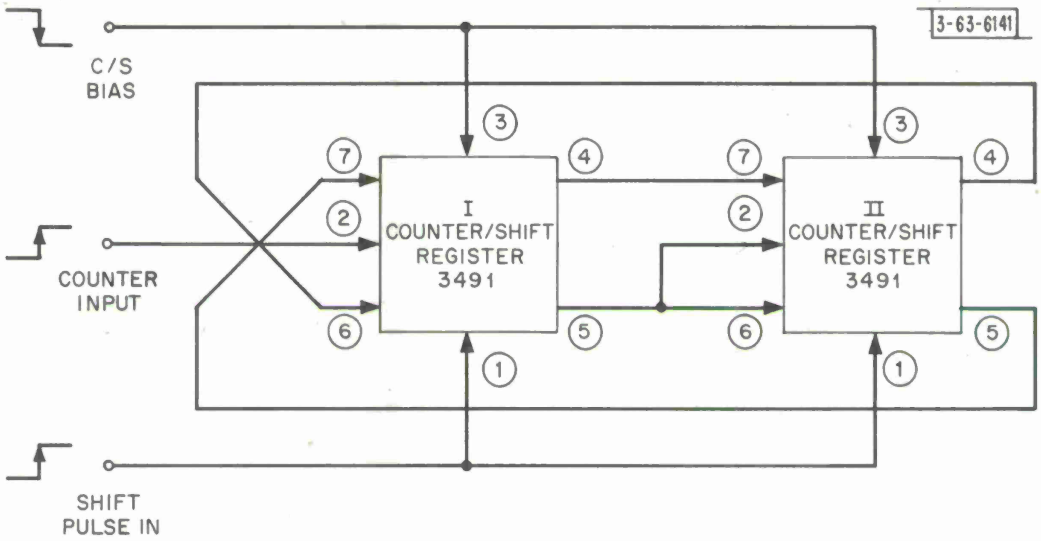
3-63-6140


COUNTER TRIGGERING - PULSE AMPLITUDE vs FREQUENCY
CURVE B
PULSEWIDTH: 50 µsec
t_r: 100 nsec
INPUT PULSE AMPLITUDE (volts)
FREQUENCY (kHz)
0
1
2
3
4
5
6
0.01
0.1
1
10
100

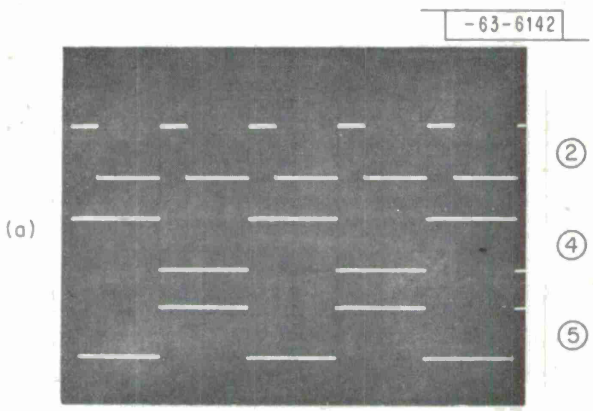

COUNTER TRIGGERING - PULSE AMPLITUDE vs PULSEWIDTH
CURVE A
FREQUENCY: 10 kHz
t_r: 100 nsec
PULSE AMPLITUDE (volts)
PULSEWIDTH (µsec)
0
2
4
6
8
10
12
1
2
3
4
5
6


SHIFT REGISTER TRIGGERING PULSE AMPLITUDE vs FREQUENCY
CURVE D
PULSEWIDTH: 10 µsec
t_r: 100 nsec
INPUT PULSE AMPLITUDE (volts)
FREQUENCY (kHz)
0
1
2
3
4
5
6
0.01
0.1
1
10
100


SHIFT REGISTER TRIGGERING PULSE AMPLITUDE vs PULSEWIDTH
CURVE C
FREQUENCY: 10 kHz
t_r: 100 nsec
PULSE AMPLITUDE (volts)
PULSEWIDTH (µsec)
0
2
4
6
8
10
12
1
2
3
4
5
6

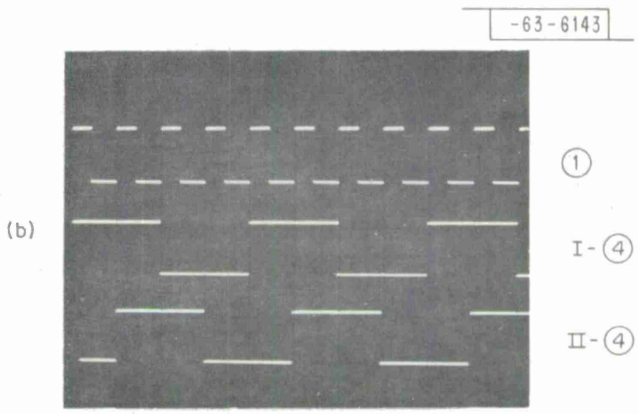


COUNTER/SHIFT REGISTER TEST APPLICATION



HORIZONTAL: 50 μsec/cm
VERTICAL: 5V/cm
WAVEFORMS AT 10 kHz

COUNTER FLIP-FLOP OUTPUT

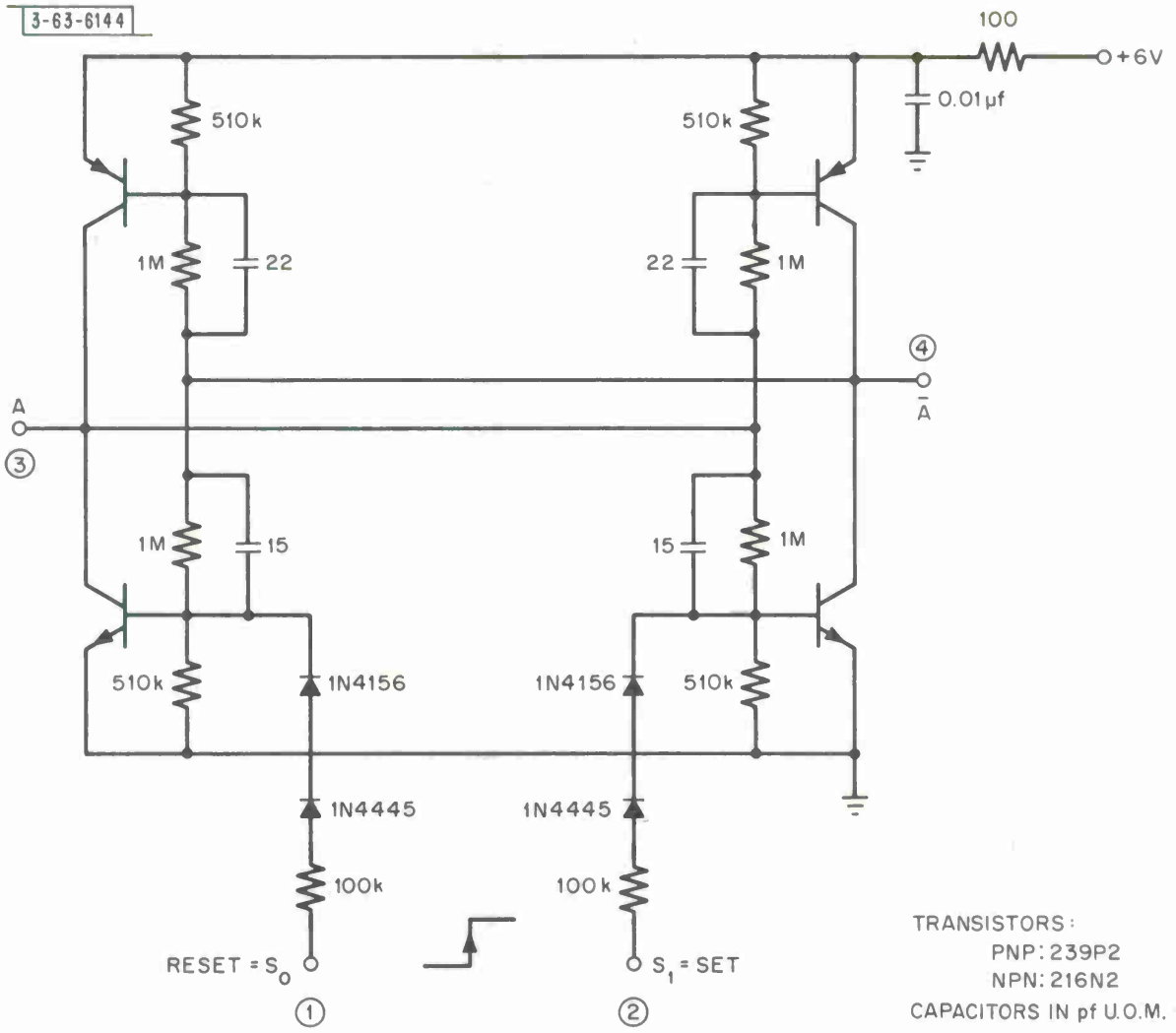


HORIZONTAL: 0.1 msec/cm
VERTICAL: 5 V/cm
WAVEFORMS AT 10 kHz

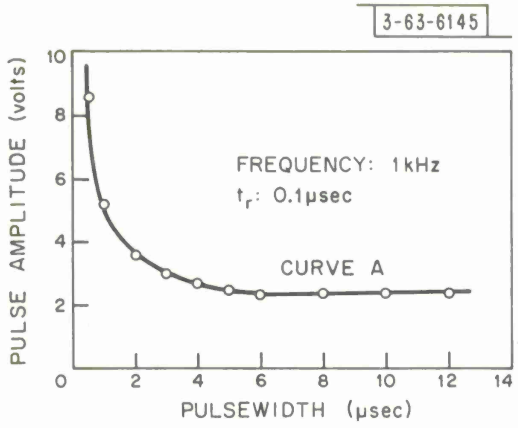
SHIFT REGISTER OUTPUT

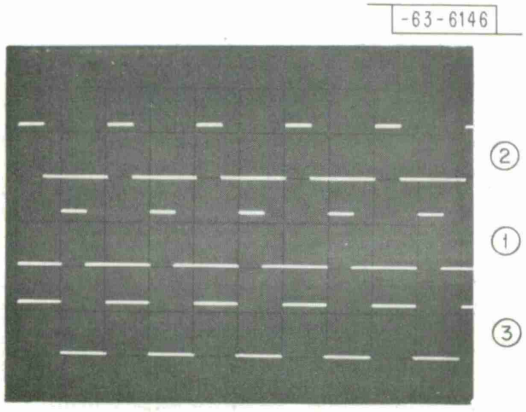
Circuit: Flip-Flop, Low-Frequency Set/Reset #3621

Operational Capabilities:	
Frequency range	0 to $\geq$10 kHz
Temperature range	$\geq \pm 50°C$
Supply voltage variation	$\geq \pm 50$ percent
Input Requirements:	
Trigger rise time	≤ 1 μsec
Pulse amplitude	Curve A
Pulsewidth	Curve A
Output Characteristics:	
Rise time	20 nsec
Fall time	30 nsec
Propagation delay	3 μsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	Standby = 60 μW
	1 kHz = 72 μW
	10 kHz = 240 μW



CIRCUIT DIAGRAM 16 (Flip-Flop, Low-Frequency Set/Reset)
MODULE # 3621

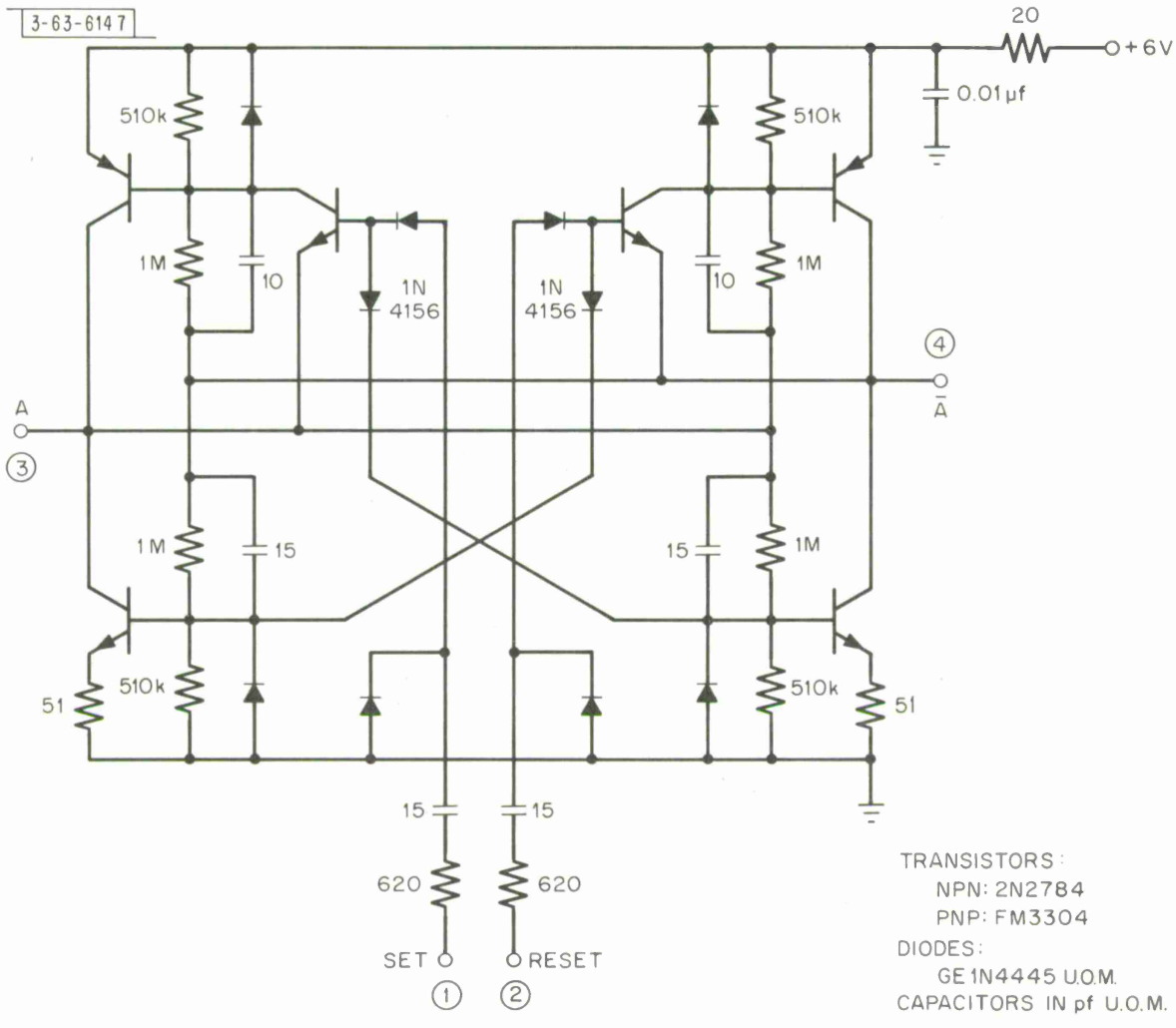




HORIZONTAL: 0.5 msec/cm
VERTICAL: 5V/cm
WAVEFORMS AT 1 kHz

Circuit: Flip-Flop, High-Frequency Set/Reset #5861

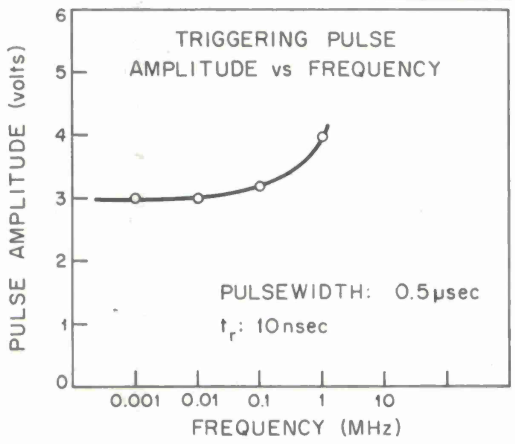
Operational Capabilities:	
Frequency range	0 to $\geq$1 MHz
Temperature range	$\geq \pm 50°C$
Supply voltage variation	$\geq \pm$ 30 percent
Input Requirements:	
Trigger rise time	$\leq$0.1 μsec
Pulse amplitude	6 volts ± 1 volt
Pulsewidth	$\geq$0.1 μsec
Pulse amplitude with frequency	Curve A
Output Characteristics:	
Rise time	$\leq$5 nsec
Fall time	$\leq$5 nsec
Propagation delay	10 nsec
Levels	$\approx$0 and +6 volts
Other Characteristics:	
Power consumption	Curve B

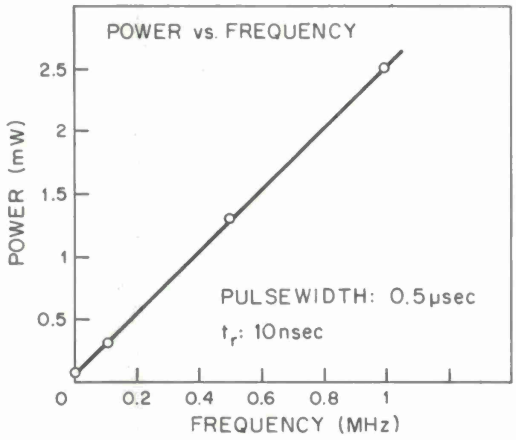


CIRCUIT DIAGRAM 17 (Flip-Flop, High-Frequency Set/Reset)
MODULE #5861

#5861

3-63-6148





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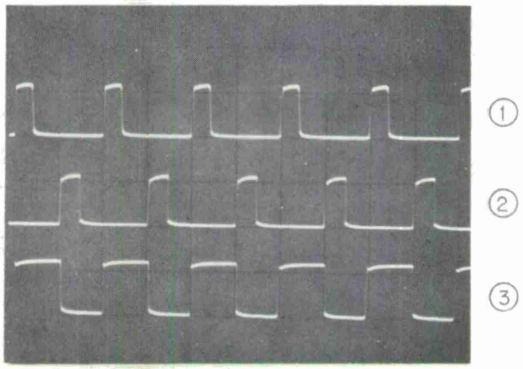

HORIZONTAL: 0.5µsec/cm
VERTICAL: 5V/cm
WAVEFORMS AT 1MHz

IV. DEVELOPMENT OF HIGH-SPEED, MINIMAL-POWER FLIP-FLOPS

Current and future digital system designs for space applications require an increasing amount of high-speed, minimal-power flip-flop circuit configurations to perform on-board real-time signal processing tasks. Many operational requirements are placed on such circuits, including:

(a) Long-term stability and reliability,
(b) Spurious noise immunity,
(c) Insensitivity to voltage transients and variations,
(d) Wide operational temperature range,
(e) High-speed capability,
(f) Minimal power consumption,
(g) Low-temperature positive start-up,
(h) Minimum use of supply voltages.

Of the above requirements, high speed and minimal power present the greatest design challenge.

The developments contained herein are the result of an objective to investigate various flip-flop configuration and gating techniques to determine which approach best satisfies the list of requirements. A secondary objective was to determine which configuration-gating technique could be used to make the combination most adaptable to performing the various digital system functions required of a flip-flop circuit and still remain within the bounds of the previously listed requirements.

Considerable experimentation using various configuration-gating techniques has been carried out to evaluate speed-power efficiency, as well as the other requirements. From the results of these experiments, a set of design procedures can be set forth which take the form of an "efficiency format." These procedures are meant to bring to light the areas where design adjustments can be instrumental in arriving at the operational requirement levels of speed, power, etc. Following a listing of these procedures, each will be discussed in more detail.

Results of these efforts have produced the circuit configurations shown in Sec. III as module numbers 3811, 3751 and 5861.

A. Design Guides for Developing High-Speed, Minimal-Power Flip-Flop Circuits

(1) Choose as a basic flip-flop configuration, one with low standby power and high switching efficiency.

(2) Utilize low-capacitance, ultra-fast switching transistors whose parameters are based upon minimums of collector current.

(3) Reduce cross-coupling capacitor values to operational minimums, maintaining reliability throughout the applicable temperature range.

(4) Use an input circuit which employs series limiting, capacitive trigger coupling and rectification of the unnecessary input signal excursion.

(5) Choose a gate configuration which performs steering and triggering functions based upon minimum switching excursions and does not employ physical capacitors.

(6) Install low-capacitance, fast-recovery type clamp diodes, where necessary, for the prevention of charging or discharging shunt capacities or physical capacitors through larger-than-necessary voltage excursions.

(7) A primary design objective should be the reduction of total circuit capacitance to an absolute minimum.

(8) Decoupling networks should be installed on voltage supply busses.

B. Circuit Development Incorporating the "Efficiency Format" Basic Configuration

The flip-flop configuration most generally suitable for high-speed, minimal-power applications using discrete components is the complementary current demand type* shown in Fig. 4. It is used in this application because of such advantages as:

(1) Low, adjustable standby power,

(2) Saturated transistors provide fixed voltage level outputs,

(3) Output current limited only by collector current available,

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* R. H. Baker, "Maximum Efficiency Transistor Switching Circuits," Technical Report 110, Lincoln Laboratory, M.I.T. (22 March 1956), DDC 96497.

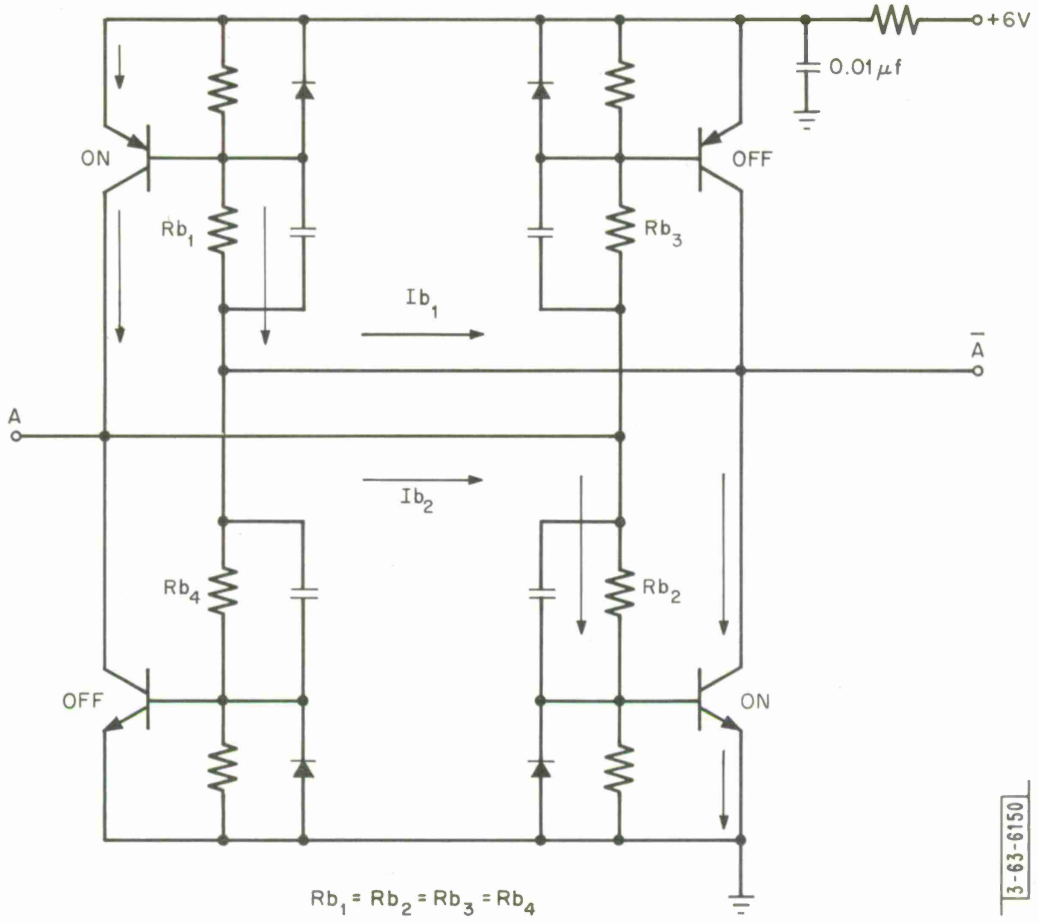

Fig. 4. Basic complementary flip-flop circuit.

(4) Output rise and fall times are inherently fast,
(5) Relatively insensitive to supply transients and variations,
(6) Long term reliability and stability,
(7) Component tolerances are not critical,
(8) Adaptable to many triggering variations,
(9) Requires only one supply voltage.

The standby power level of a flip-flop configuration such as that of Fig. 4 can be adjusted to be very low. Ib_1 and Ib_2 are essentially the only currents flowing for a given standby condition. Therefore, standby power is only being dissipated in two base resistors, in this case Rb_1 and Rb_2. The base resistors therefore directly determine the standby power level which will approximate

$$P_{STBY} \approx 2Ib^2Rb$$

To uphold transistor parameters that are dependent upon collector current, which is determined by the base resistors, enough collector current must be provided to insure good transistor operation for any given application. This then is the factor limiting how much the standby power can be reduced.

The requirement that standby power be low is justified for a flip-flop circuit that is functioning as a binary storage element. It is also justified for flip-flops used in other configurations, such as counter-storage elements. For storage purposes, the flip-flop will be running at a very low power level. However, when the triggering speed of the counter reaches 10 kHz and above, standby power begins to be a less significant contributor to total power consumption, and transition power begins to increase. Transition power will be discussed in Sec. F below. When a flip-flop is used for continuous high-speed counting, such as in a frequency divider application, standby power can be increased thereby increasing collector current which will allow higher speed capabilities to be reached.

C. Transistor Requirements

The transistors making up the basic flip-flop in Fig. 4 should be of the low-capacitance, low-current, ultra-fast switching type which inherently produces

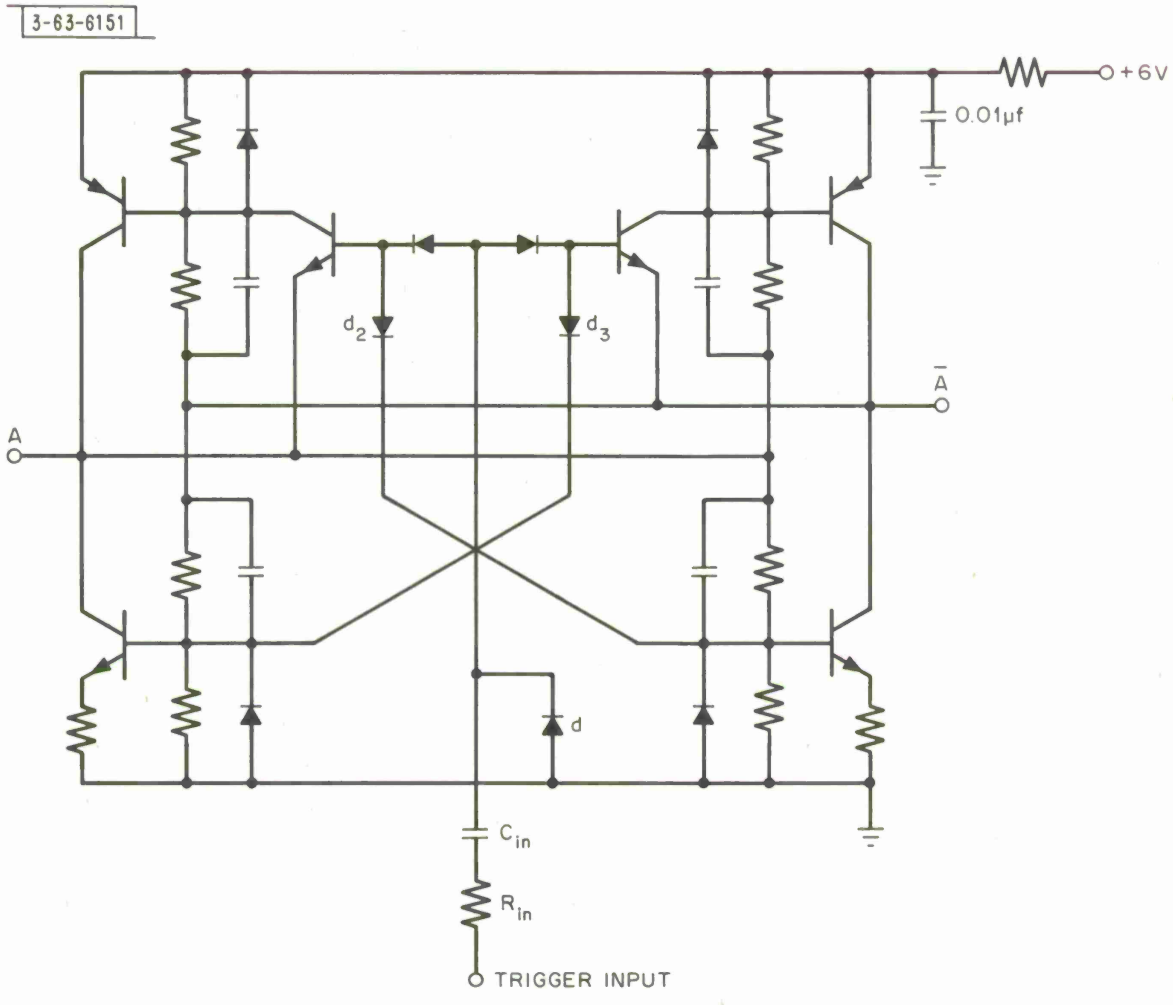

Fig. 5. Input circuit for trigger gate.

fast turn-on, turn-off characteristics and has very short storage time. With transistors such as this in the circuit, the switching current requirements are reduced and transition time is shortened. All this results in lower transition power and a higher speed capability.

These requirements also apply to any transistors used in gating circuitry. Besides quick-acting gating functions being assured, input drive requirements can be lowered resulting in an input power reduction.

D. Cross Coupling

Cross coupling is established by means of the capacitors shunting the base resistors shown in Fig. 4. With the application of a trigger signal, the flip-flop begins to reverse state. Current pulses formed by these capacitors, from the high-speed voltage excursions of saturating transistors, help to speed the transition from one bistable state to the other by turning transistors on and/or off as required. The switching sensitivity of the four basic configuration transistors largely determines the size requirement of the speed-up capacitors, which should be left as small as possible. Large speed-up capacitors result in increased time constants that inhibit high-speed operation, and in longer transition times that cause transition power consumption to increase. Small speed-up capacitors also serve to reduce the circuits' sensitivity to spurious noise, thus promoting greater stability.

E. Input Circuit

Figure 5 shows a complete flip-flop circuit configuration including a counting gate. R_{in}, C_{in} and d comprise the input circuit to this gate. R_{in} serves the purpose of adjusting the input sensitivity of the circuit to spurious noise and/or trigger signal level. A dual function is to limit the input current passed by C_{in}, thereby reducing the drive power requirement. Capacitive coupling of the triggering signal prevents direct current from being drawn from triggering circuitry and allows the gate to be driven at higher speeds. C_{in} should be no larger than necessary to accomplish stable triggering. As a result of the input capacitor, positive and negative voltage excursions are formed from

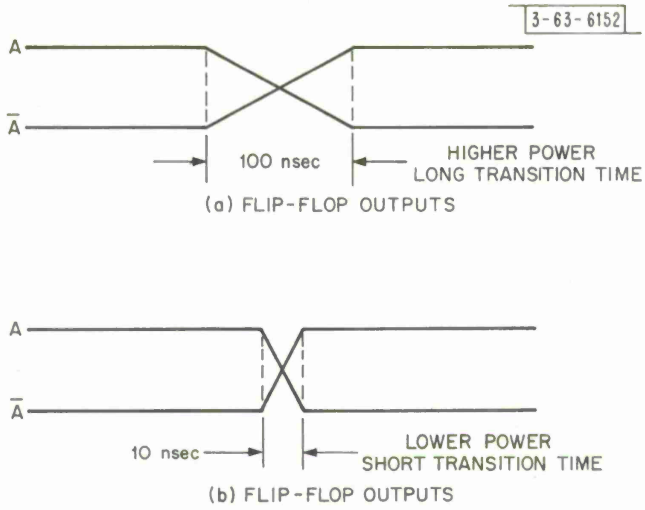

Fig. 6(a-b). Relative transition time vs power.

the trigger pulse. To promote greater speed and to conserve power, the unused excursion should be eliminated by rectification. The charge-discharge potential of C_{in} is thus lessened.

F. Gating Circuitry

The manner in which various gating functions are performed is of great importance in high-speed, minimal-power applications. Operational characteristics that are largely a result of the gating technique used are:

(1) Speed capability,
(2) Transition time,
(3) Transition power.

The speed capability is largely dependent upon the reaction time of the steering portion of the gate circuit and the time delay between the input trigger signal and the output transition. Avoiding the use of nodal voltages derived from resistive current flow, for steering purposes, greatly decreases the reaction time of the steering mechanism. To reduce propagation delay, direct vs capacitive coupling should be used. In this way, capacitor charge-discharge times are eliminated. Another advantage derived from eliminating gate-coupling capacitors is that charge requirements which would otherwise be present are reduced and less switching current is required.

Transition time is the time required to switch from one bistable state to the other, and is a resultant of the gating technique combined with cross-coupling capacitor action. During this time, all transistors of the flip-flop are in the process of being switched on and/or off, resulting in current being dissipated throughout the circuit. Any means whereby this "dissipation" time can be shortened should certainly be introduced. As an example, in Fig. 5 diodes d_2 and d_3 provide a current pulse, derived from the input, that serves to precharge the total base circuit capacitance of the off NPN that is about to be turned on, thereby promoting a faster transition. Figure 6(a-b) depicts extreme cases of transition time vs power consumption. Short transition times help to conserve power and to increase the potential frequency capability of the flip-flop.

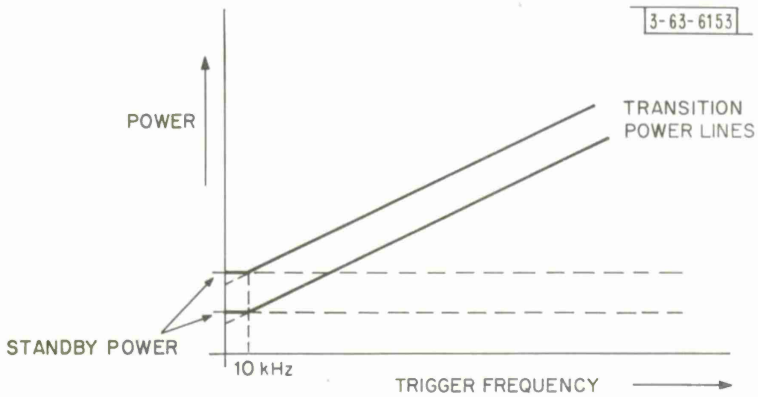

Fig. 7. Relative transition power vs standby power.

When the rate at which a flip-flop is to be switched is increased, an increase in power consumption can be expected. This is inevitable due to the fact that a dissipation factor is required to effect each transition that is to occur. This dissipation factor can be called switching, or transition, power and is a result of all of the individual dissipations that take place during a transition. For the most part, these individual dissipations are due to circuit capacitance charge requirements, transistor saturation requirements, diode IR drops, and transistor conduction during transition time. Transition power begins to become significant when the triggering speed surpasses 10 kHz and increases linearly with frequency throughout the useful range of the flip-flop. In Fig. 7, examples of transition power lines are shown relative to standby power.

It is apparent that reduced power levels at high frequencies can only be attained by reducing the slope of the transition power line, which, in effect, means eliminating dissipation factors that occur in the process of switching.

G. Clamp Diodes

Excessive voltage excursions should be eliminated wherever possible so that capacitor charge-discharge requirements and relatively long time constants are eliminated or reduced. This provision reduces transition time and power, and increases the frequency capability of the flip-flop. Diodes of low capacitance and fast recovery are recommended in order not to increase significantly total circuit capacitance and to reduce secondary time constants.

H. Circuit Capacitance

Much emphasis has been placed upon eliminating and/or reducing capacitors and total circuit capacitance when and where it is operationally possible. This emphasis is justified by the fact that charge requirements of capacitors, and circuit capacitance in general, account for a major portion of the transition power that a circuit dissipates. For speed purposes and switching current requirements due to transistor turn-on, turn-off and storage characteristics, "speed-up" capacitors are necessary and amount to approximately 70 percent of the total circuit capacitance. The remainder of the total circuit capacitance

includes the input capacitor, the internal capacitance of transistors, component shunt capacities, and stray capacitance due to lead length and wiring. It is theoretically impossible to reduce total circuit capacitance to zero. However, good design procedures and proper selection of circuit transistors and components will result in reducing the total circuit capacitance to a minimum.

I. Supply Voltage Decoupling

The application for which circuits of this type are designed requires that they be stable and reliable and yet maintain a degree of sensitivity in order to perform as required. Triggering sensitivity must be maintained, but at the same time the circuit stability must be upheld by protecting the circuit from external factors that could cause false triggering. In this regard, individual decoupling networks on circuit supply voltages serve a dual purpose. Voltage supply busses in digital systems, where these circuits are used, are generally prone to transients which are caused by nature of the random current demands made on the supply voltages by the many switching circuits and changing load conditions. The isolation provided by a decoupling network helps to protect the circuit from these system buss transients. Conversely, any transients that would otherwise be developed by the circuit itself are suppressed, thus maintaining a level of "cleanliness" at the supply busses.

J. Summary

In most digital systems, flip-flop circuits make up a large portion of the total circuit complement and can potentially use a large portion of available power. Attaining goals whereby minimal-power flip-flops result can greatly increase the performance capacity of a given system. Foremost in importance in circuits for space applications is that the standby power requirement be minimal. When this requirement is fulfilled, additional "system design room" results. Secondly, speed-power factors must be maintained at a minimum to afford flexibility.

The development of an integrated circuit based on the circuit of Fig. 5 is hoped for. This would result in a flip-flop having the advantages of low standby power, low speed-power factor, high-speed capability and small-size package.

V. CONCLUSION

Work resulting in the information contained in this report has been performed as an aid to the systems designer as well as to others seeking knowledge concerning circuit operation and use.

Incorporating circuit elements whose capabilities and requirements are well-defined normally results in system designs which are potentially more trouble free, thus serving to make operational and environmental system checkout less demanding.

It is hoped that the guide lines presented in Sec. IV will be useful in the transformation from discrete component circuitry to integrated circuits that are specifically manufactured for space systems applications.

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13. ABSTRACT

This report contains various configurations of operational low-power digital circuit elements which have been refined and/or developed to carry out many functional requirements of digital system designs. Although they are primarily intended for use in space-oriented digital system applications, e.g., the Lincoln Experimental Satellite (LES) program, the configurations need not be limited to this purpose.

Characteristic operational data are included in all cases to point out various circuit requirements, capabilities and limitations.

A myriad of flip-flop configurations is provided to promote efficient systems design in regards to power consumption, noise immunity and cost.

Section IV covers some design considerations relating to high-speed, low-power flip-flop development.

14. KEY WORDS

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